CHA6551-99F

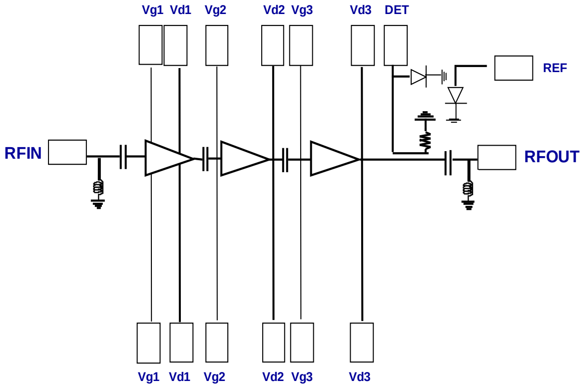
17-24GHz Power Amplifier

GaAs Monolithic Microwave IC

Description

The CHA6551-99F is a three stage monolithic GaAs high power circuit producing 1.6 Watt output power.
It is highly linear, with possible gain control and integrates a power detector. ESD protections are included.
It is designed for a wide range of applications: Space, military and automotive communication systems

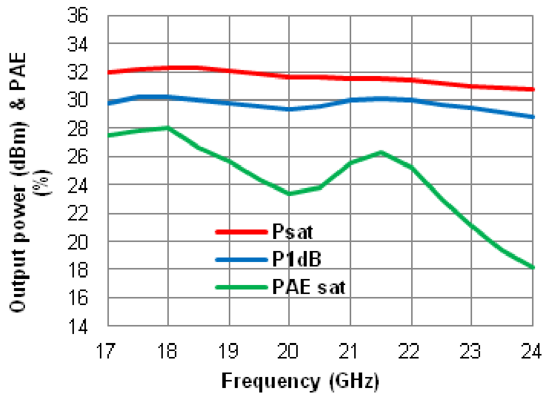
The circuit is manufactured with a pHEMT process, 0.15µm gate length.



Main Features

- ■ Broadband performances: 17-24GHz
- ■ 32dBm saturated power
- ■ 39dBm OIP3
- ■ 22dB Gain
- ■ DC bias: Vd = 4.0 Volt @ Id = 880mA
- ■ Chip size 3.60x3.46x0.07mm

Output Power & PAE vs frequency



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17		24	GHz
Gain	Linear Gain		22		dB
Psat	Saturated output power		32		dBm
OIP3	Output IP3		39		dBm

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Specifications

Tamb.= +25°C, Vd = +4V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17		24	GHz
Gain	Linear Gain		22		dB
ΔG	Gain variation in temperature		± 0.03		dB/°C
Psat	Saturated Output Power		32		dBm
OIP3	Output IP3		39		dBm
P1dB	Pout at 1dB of compression		30		dBm
PAE	PAE at saturation		25		%
CG	Gain control range		15		dB
NF	Noise Figure		5		dB
RlIn	Input Return Loss		15		dB
Rlout	Output Return Loss		15		dB
Dr	Detection dynamic range(for output power detection up to Psat)		30		dB
Vdetect	Voltage detection $V_{REF} - V_{DET}$ up to Psat		10 to 1500		mV
Vg	DC gate voltage		-0.70		V
Id	Total drain current		880		mA

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Absolute Maximum Ratings [1] [2]

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6	V
Id	Drain bias current	1900	mA
Vg	Gate bias voltage	-2 to +0	V
Vdg	External drain-gate excursion	12	V
Pin	Maximum peak input power overdrive	+20	dBm
Tj	Maximum Junction temperature	175	°C

[1] Operation of this device above anyone of these parameters may cause permanent damage.
[2] These are stress rating only, and functional operation of the devices at these conditions is not implies.

Recommanded Operating Range [3] [4]

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4 to 5.5	V
Id	Drain bias current	880 to 1150	mA
Vg	Gate bias voltage	-2 to 0	V
Pin	Maximum peak input power overdrive	20	dBm
Ta	Operating temperature range	-40 to 95	°C

[3] Electrical performances are defined for specified test conditions
[4] Electrical performances are not guaranteed over all recommended operating conditions.

Temperature Range

Ta	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd1	DC Drain voltage 1st stage	4V	V
Vd2	DC Drain voltage 2nd stage	4V	V
Vd3	DC Drain voltage 3rd stage	4V	V
Vg1	DC Gate voltage 1st stage	-0.70	V
Vg2	DC Gate voltage 2nd stage	-0.70	V
Vg3	DC Gate voltage 3rd stage	-0.70	V

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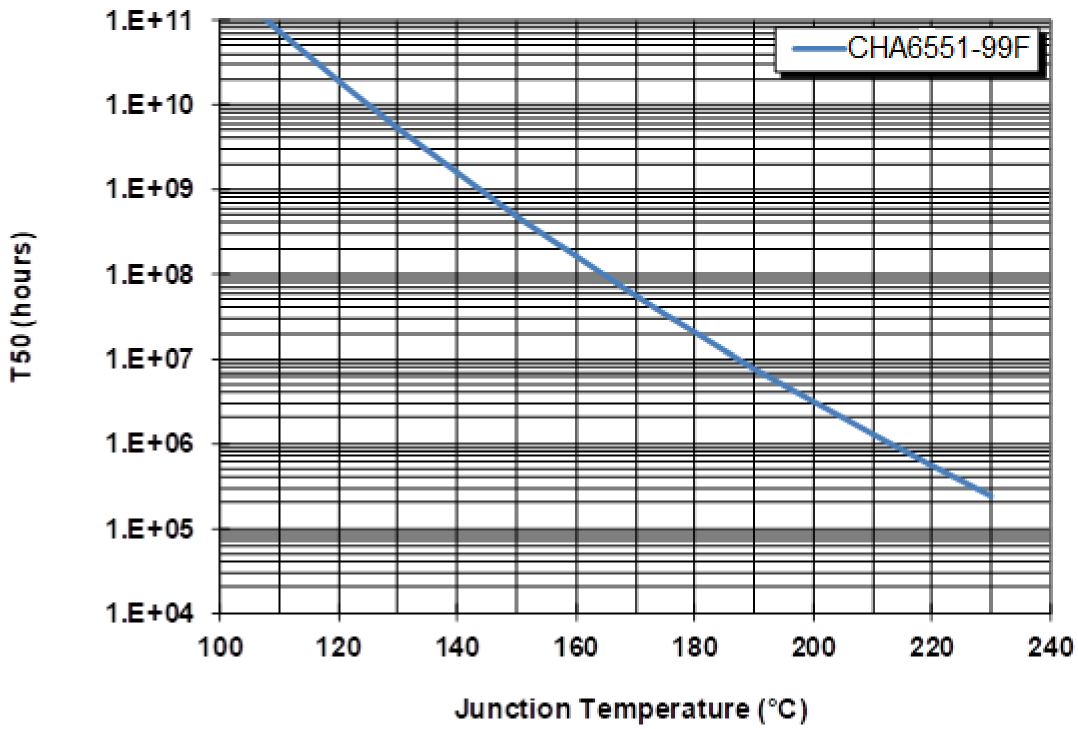
Device thermal performances

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
The temperature Tb $_{chip}$ is defined as the chip back side temperature.
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the PCB system must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	RTH (°C/W)	T50 (hours)
RTH [1] Thermal Resistance (Back of the chip)	Vd= 4V Id= 880mA Pdiss= 3.2W	125	12.5	1.0E+10

[1] Assuming 85°C Tb $_{chip}$



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Typical on-wafer Sij parameters (Pulsed mode)

Tamb.= +25°C, Vd = +4V, Id = 880mA, Pulse width = 25µs, Duty cycle = 10%

Freq (GHz)	S11 (dB)	PhS11 (°)	S21 (dB)	PhS21 (°)	S12 (dB)	PhS12 (°)	S22 (dB)	PhS22 (°)
1	-0.4	169.2	-90.8	-40.5	-87.5	97.8	-0.4	169.1
2	-0.4	158.4	-102.4	148.9	-93.4	-171.4	-0.4	158.1
3	-0.5	147.5	-72.3	161.6	-81.6	-97.2	-0.5	146.8
4	-0.5	135.9	-57.8	90.4	-83.9	52.5	-0.6	134.9
5	-0.6	123.7	-45.3	-16.9	-79.4	-170.1	-0.7	122.2
6	-0.7	110.1	-37.2	-116.8	-80.4	177.7	-1.0	108.6
7	-1.0	95.1	-33.5	137.4	-77.8	163.5	-1.4	94.1
8	-1.7	79.2	-34.0	36.9	-78.0	29.2	-2.1	80.4
9	-2.7	67.9	-41.5	-65.2	-69.9	176.5	-2.6	68.2
10	-2.5	57.0	-51.8	-57.5	-71.2	157.9	-2.6	55.6
11	-2.2	39.3	-58.7	-103.3	-74.2	127.4	-2.3	38.2
12	-2.2	18.5	-60.1	-13.6	-82.0	-162.2	-2.5	16.0
13	-2.9	-4.9	-74.6	159.3	-61.0	-125.3	-3.4	-9.1
14	-4.5	-27.8	-27.1	164.1	-53.6	-162.3	-5.9	-29.9
15	-6.9	-41.2	-2.0	59.2	-48.2	160.8	-7.8	-34.4
16	-8.5	-53.9	15.4	-86.5	-45.9	114.2	-8.4	-47.4
17	-9.4	-47.0	20.6	113.2	-45.7	74.3	-7.7	-51.9
18	-11.7	-60.7	21.3	-13.3	-43.8	28.8	-11.0	-76.9
19	-10.6	-49.8	20.8	-112.8	-48.5	-20.9	-11.0	-65.1
20	-10.3	-57.5	22.0	151.7	-53.4	-20.7	-11.9	-76.4
21	-11.6	-62.0	22.4	48.0	-54.6	-74.0	-14.1	-69.5
22	-10.6	-51.6	21.0	-53.6	-56.6	-94.9	-12.1	-59.7
23	-9.1	-58.2	20.0	-147.2	-51.4	-84.5	-11.0	-67.8
24	-9.6	-59.0	19.7	112.0	-48.0	-132.4	-11.7	-65.6
25	-7.0	-58.1	20.5	-3.0	-42.6	-170.5	-8.9	-62.1
26	-8.7	-74.5	14.9	-176.8	-41.9	170.5	-11.7	-82.4
27	-7.0	-69.2	0.1	65.5	-38.5	146.1	-9.8	-67.6
28	-6.5	-76.7	-14.1	-19.3	-34.9	111.1	-8.3	-73.1
29	-6.6	-82.2	-34.2	-100.6	-31.6	80.5	-8.1	-81.5
30	-6.7	-83.1	-34.4	55.9	-32.1	40.5	-8.3	-80.2
31	-6.3	-79.5	-32.9	17.9	-33.0	12.7	-7.5	-80.7
32	-5.1	-81.4	-32.9	-11.7	-33.6	-11.4	-6.7	-86.0
33	-4.2	-88.4	-34.4	-36.7	-34.3	-32.3	-7.0	-91.0
34	-3.8	-93.9	-34.0	-50.7	-33.1	-47.8	-7.3	-86.5
35	-3.3	-100.2	-35.4	-85.9	-34.6	-86.7	-5.3	-81.6
36	-3.3	-107.0	-36.3	-98.4	-36.2	-102.6	-3.6	-91.7
37	-3.1	-114.0	-38.5	-134.8	-37.4	-134.5	-3.3	-102.7
38	-3.4	-120.0	-45.2	-172.8	-45.9	-171.3	-3.2	-109.3
39	-3.7	-125.0	-45.7	-171.3	-46.7	-172.1	-3.3	-116.4
40	-3.8	-134.8	-49.5	177.9	-48.5	171.5	-3.4	-123.3

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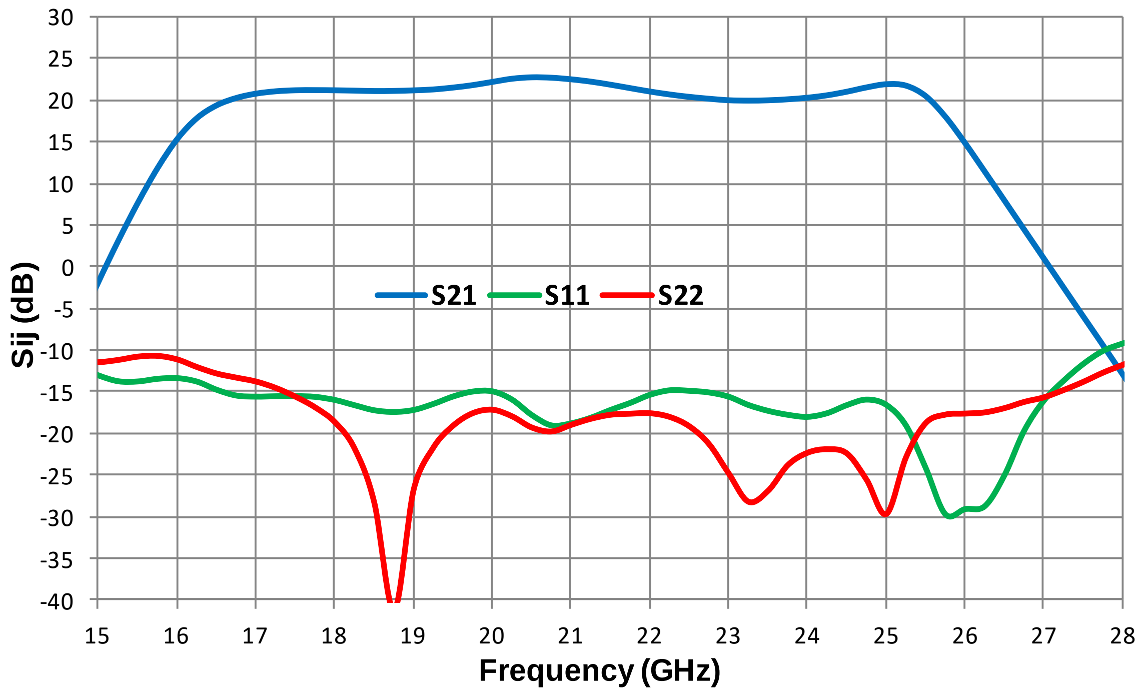
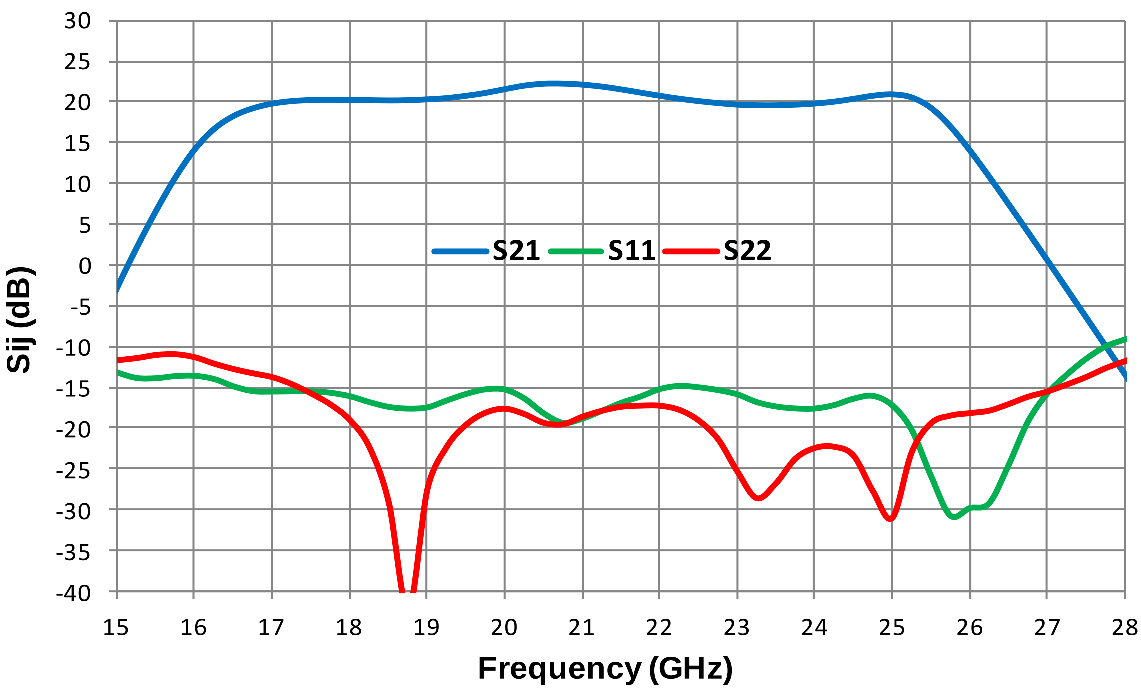
Typical Board Measurements

Tamb.= +25°C. Vd = +4V. Id = 880mA & Vd = +5.5V. Id = 1150mA
Measurement performed in the access plans of the die.

Gain & Return Losses versus Frequency
Vd = +4V. Id = 880mA



Gain & Return Losses versus Frequency
Vd = +5.5V. Id = 1150mA



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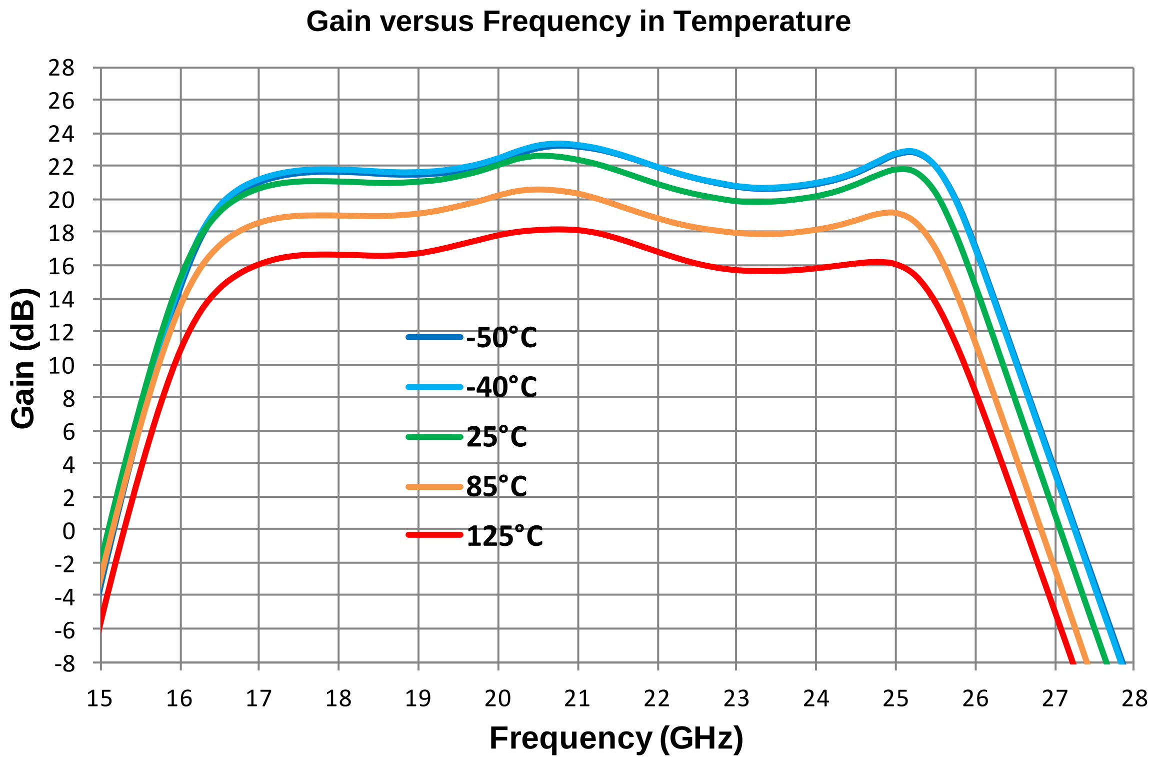

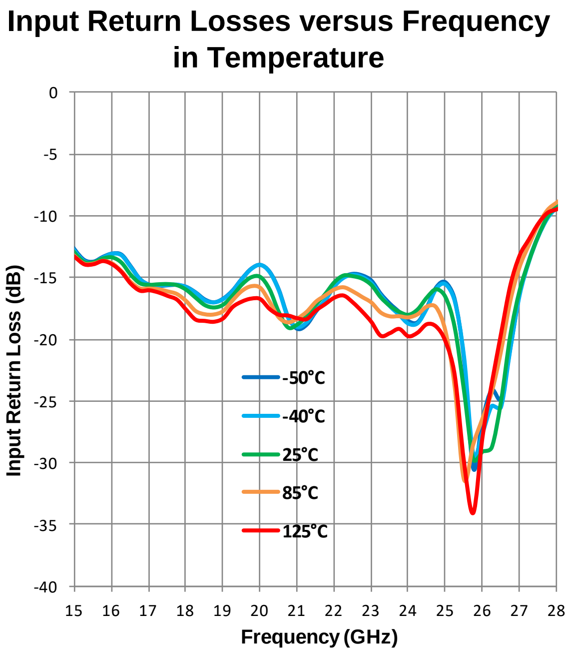

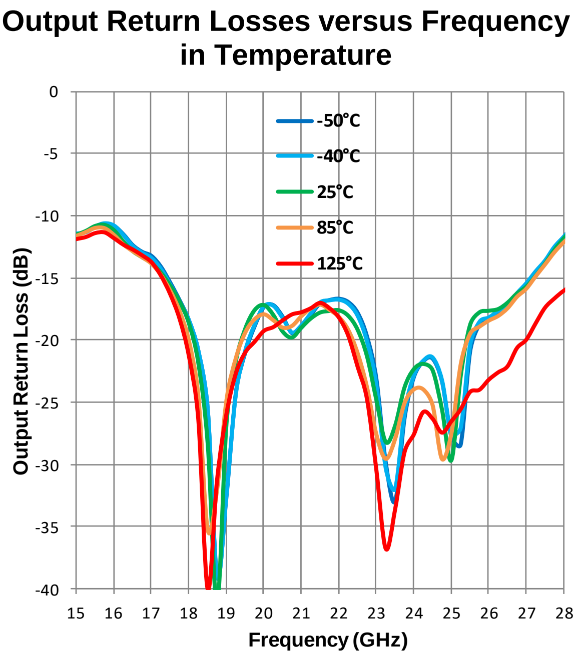

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Typical Board Measurements

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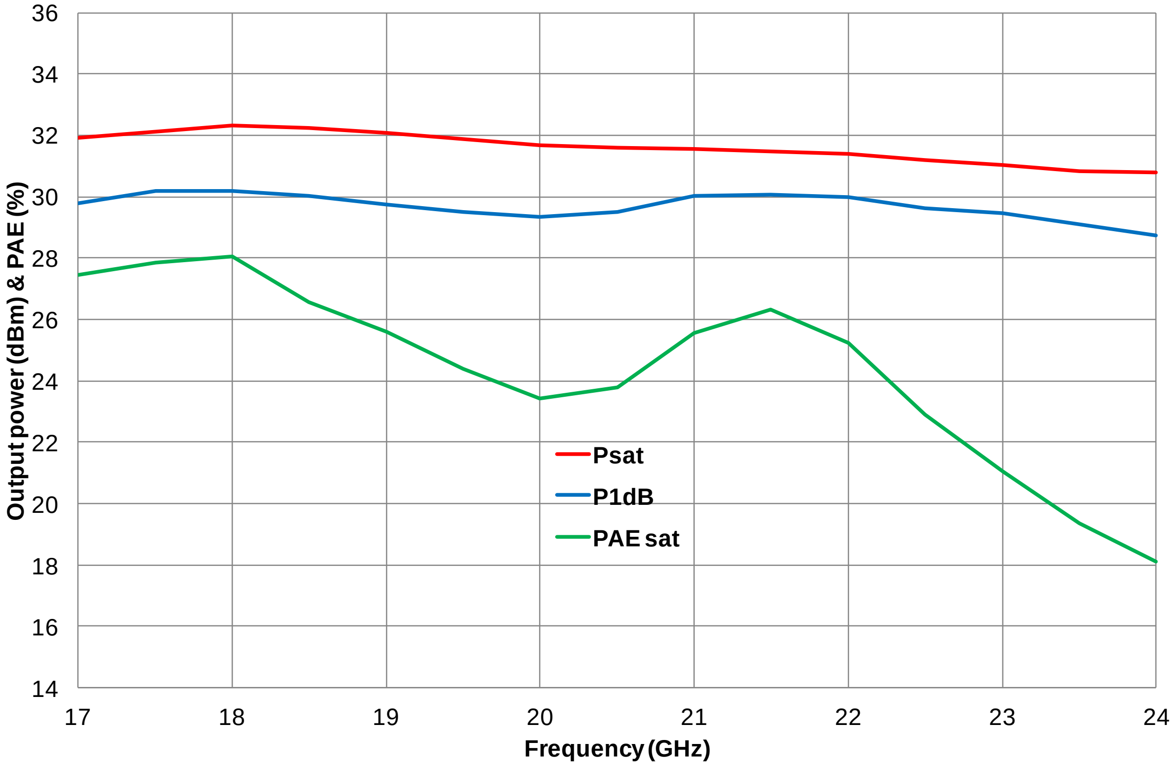
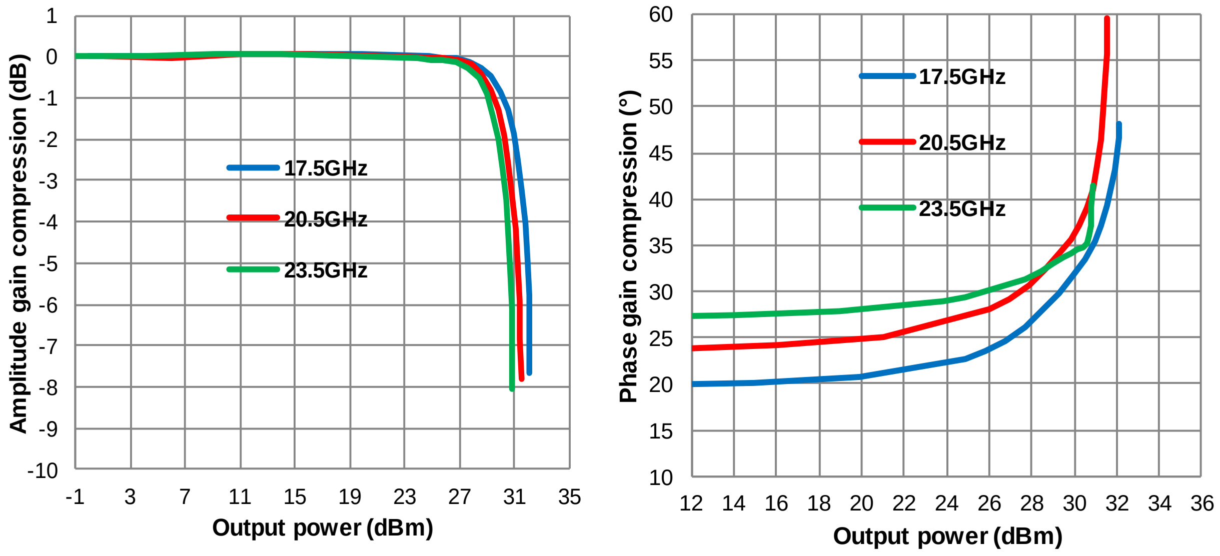
Measurement performed in the access plans of the die.

Output Power & PAE versus Frequency



Gain Amplitude & Gain Phase variation versus Output Power



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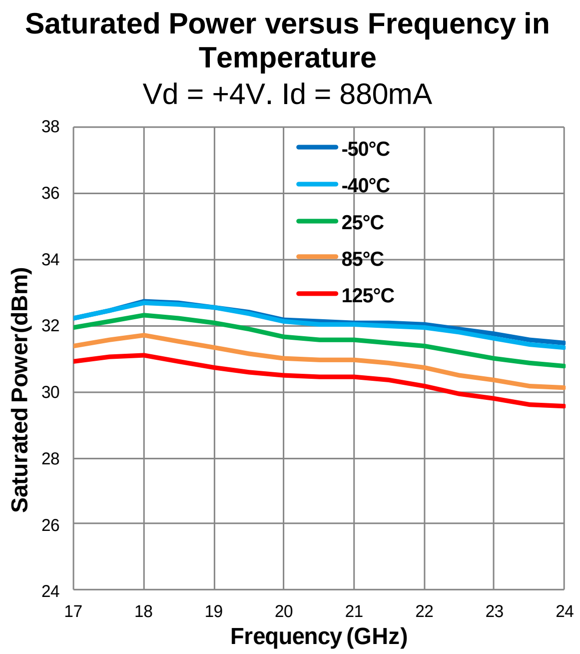

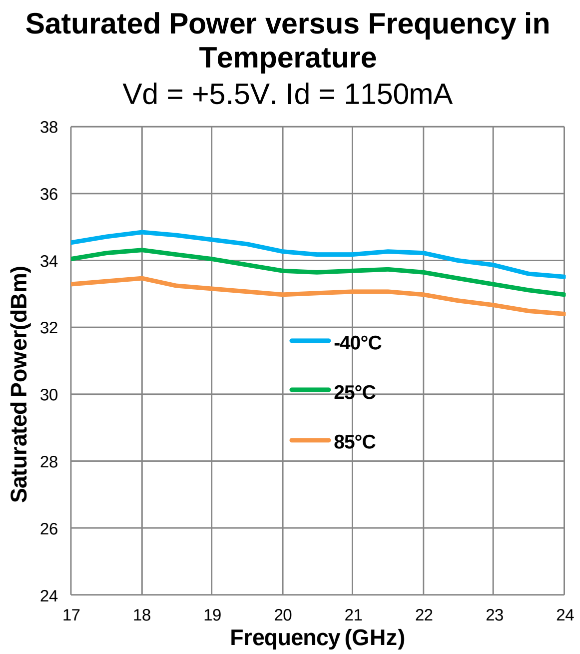

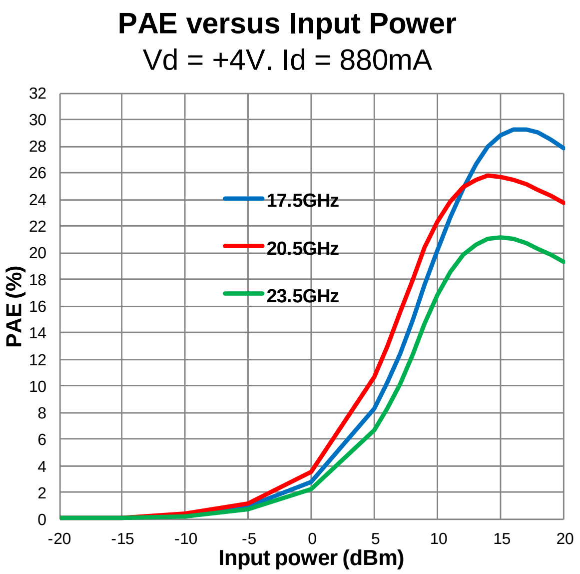

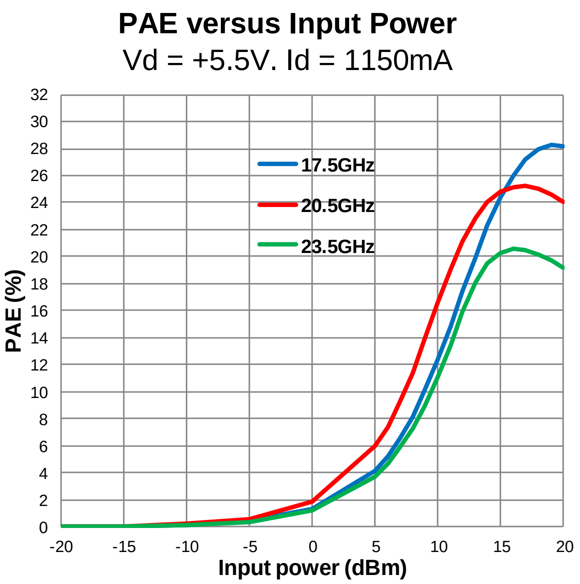

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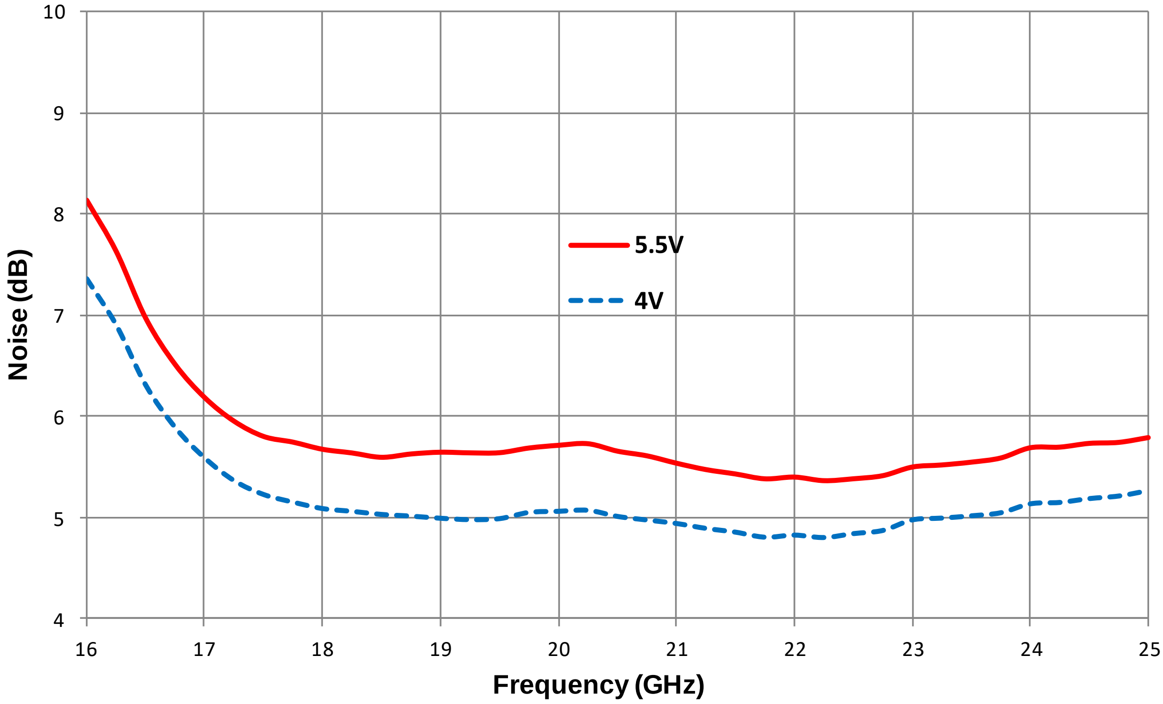
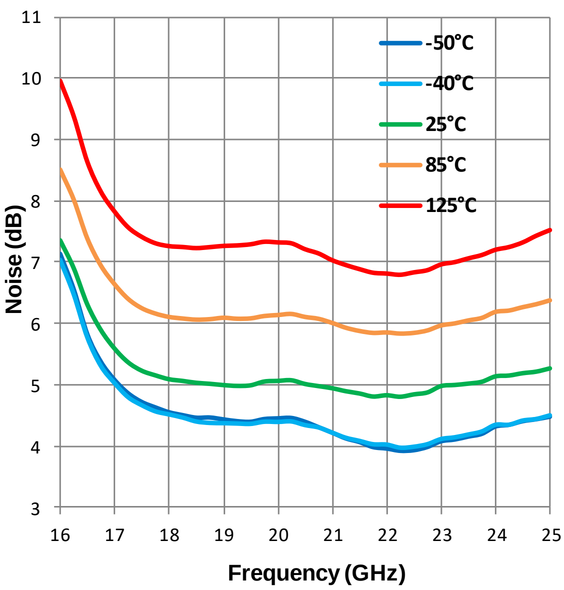
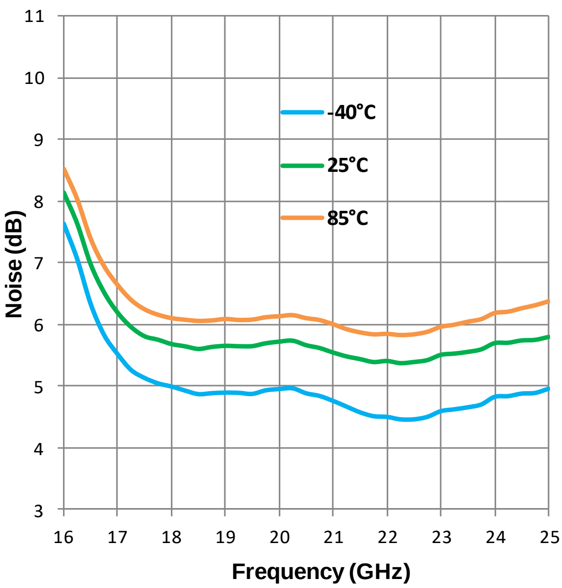
Noise Figure versus Frequency
Vd = +5.5V. Id = 1150mA
Vd = +4V. Id = 880mA



Noise Figure versus Frequency in Temperature
Vd = +4V. Id = 880mA



Noise Figure versus Frequency in Temperature
Vd = +5.5V. Id = 1150mA



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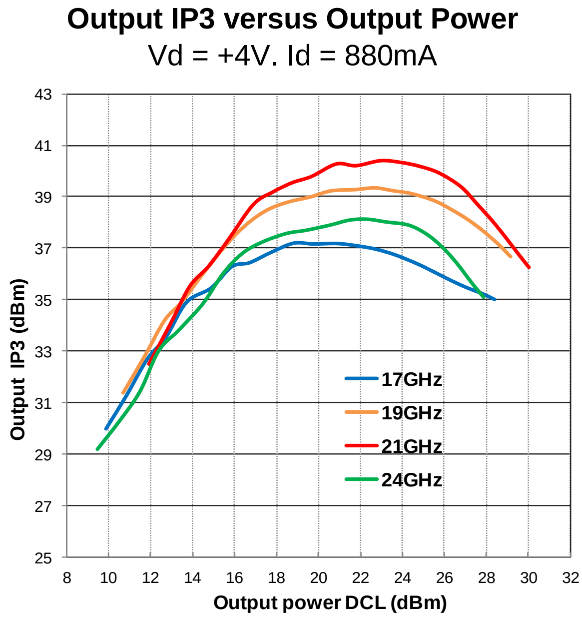

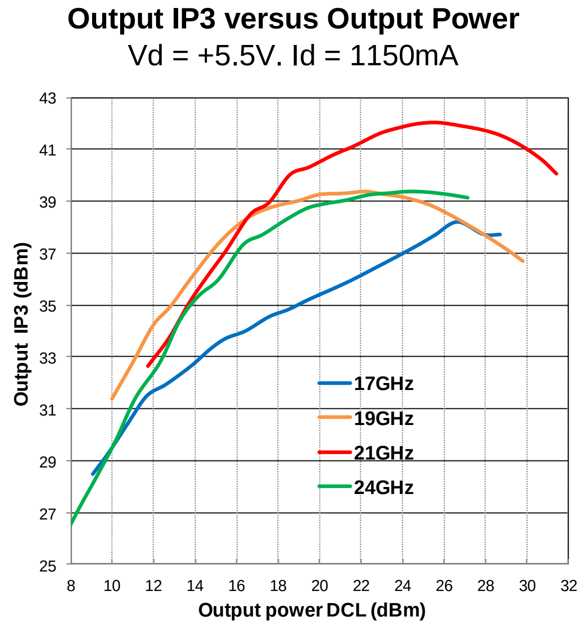

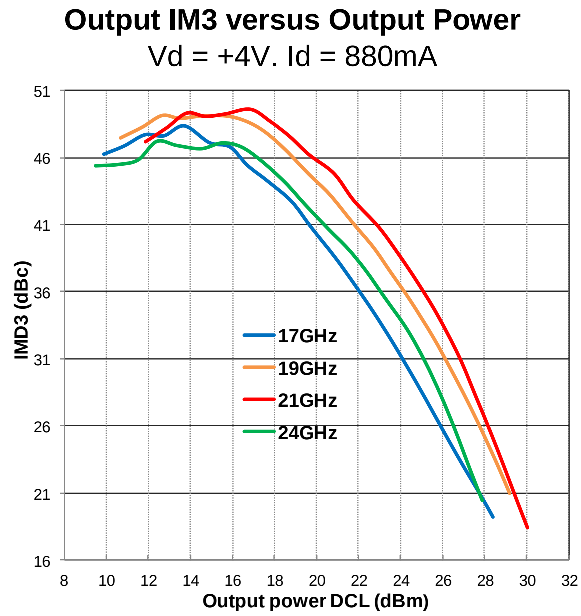

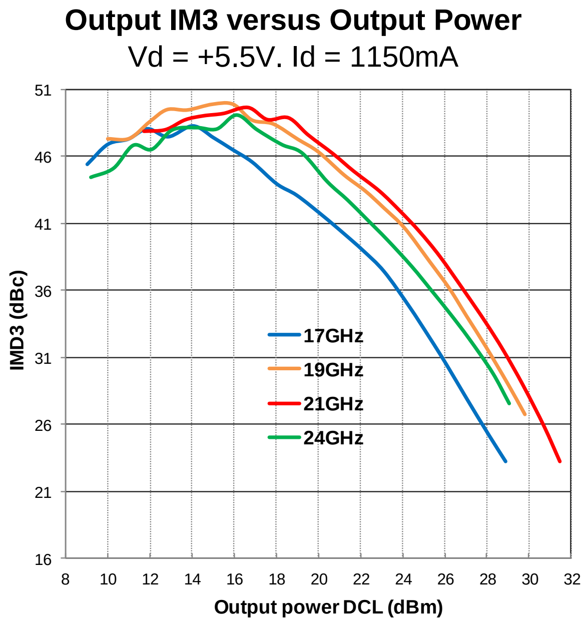

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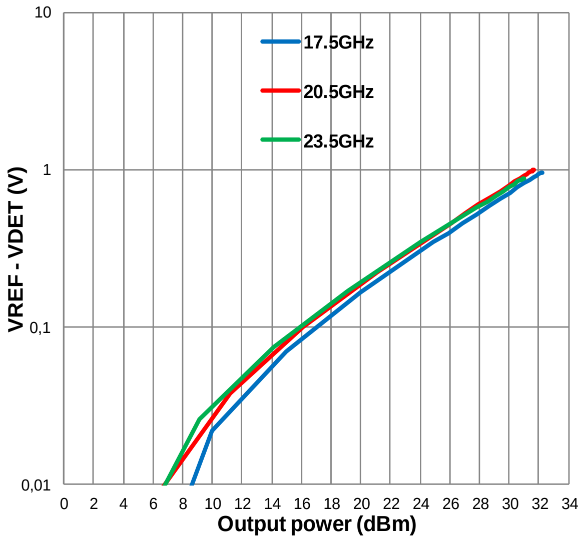
Typical Board Measurements

Tamb.= +25°C. Vd = +4.0V. Id = 880mA & Vd = +5.5V. Id = 1150mA

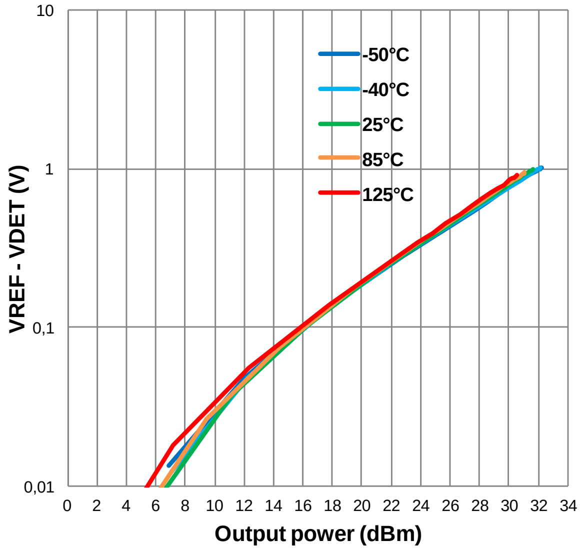
Power Detector versus Output Power

Vd = +4V. Id = 880mA



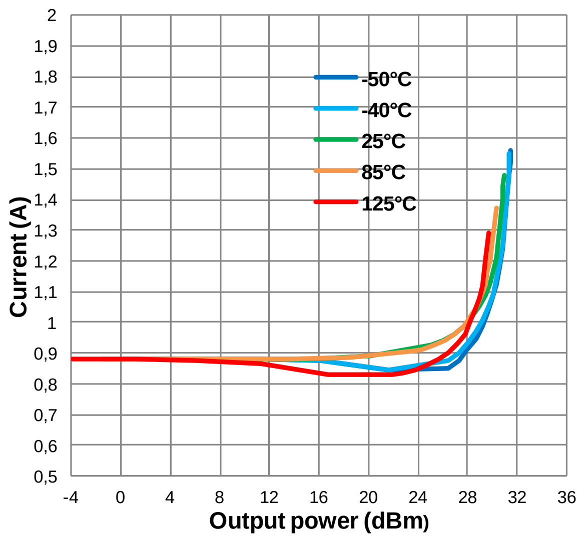
Power Detector versus Output Power & Temperature at 20.5GHz

Vd = +4V. Id = 880mA



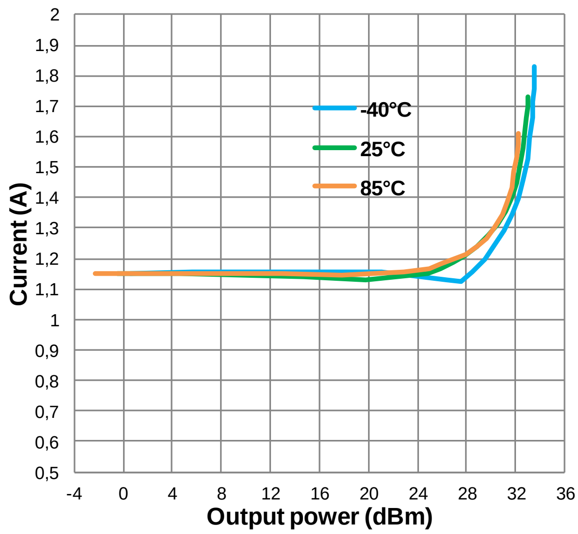
Total Drain Current versus Output Power at 20GHz

Vd = +4V. Id = 880mA



Total Drain Current versus Output Power at 20GHz

Vd = +5.5V. Id = 1150mA



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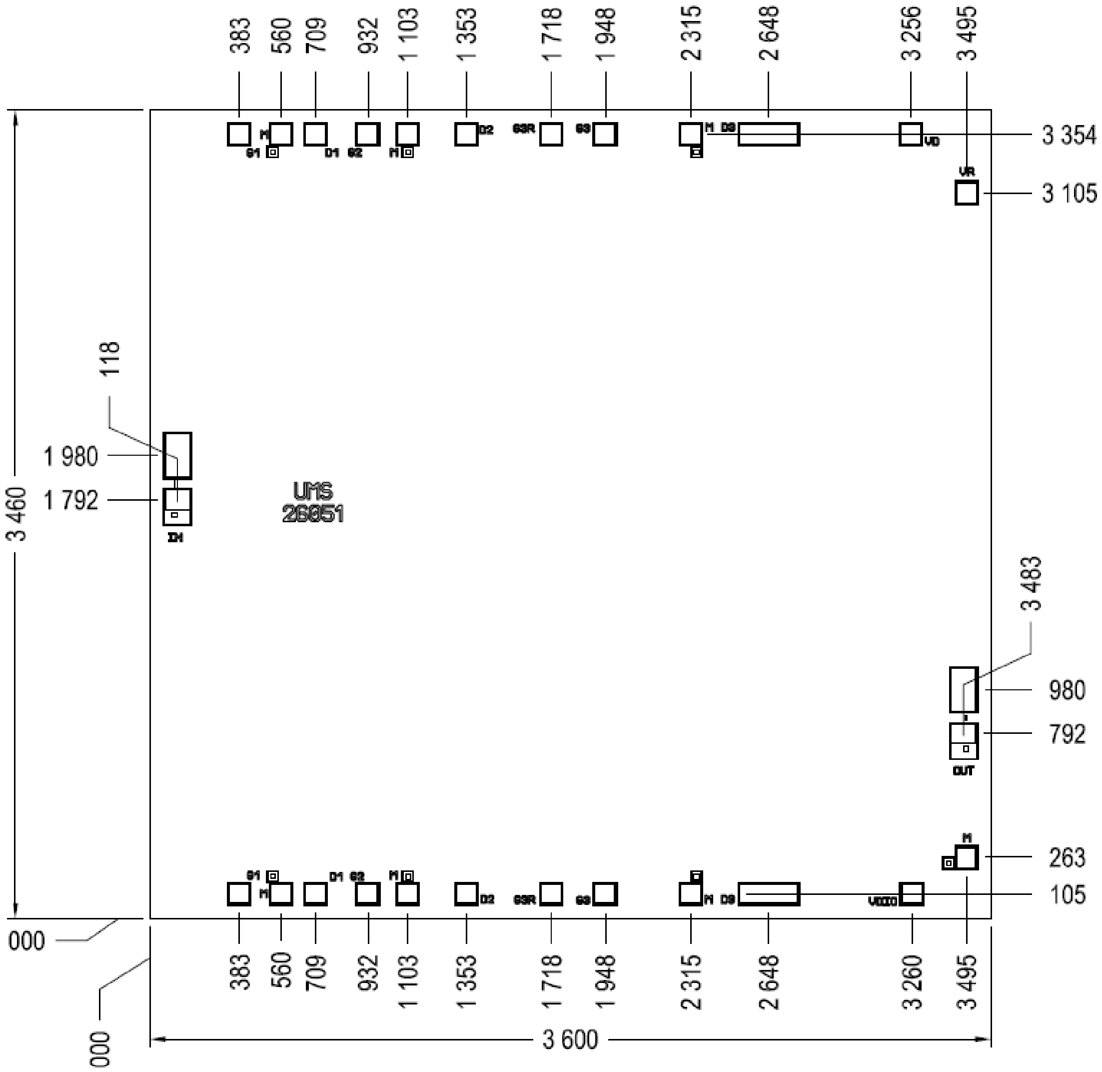
Mechanical data



Chip thickness: 70µm.
All dimensions are in micrometers
DC pad size: 83um x 83 um
RF pad size: 90um x 180 um

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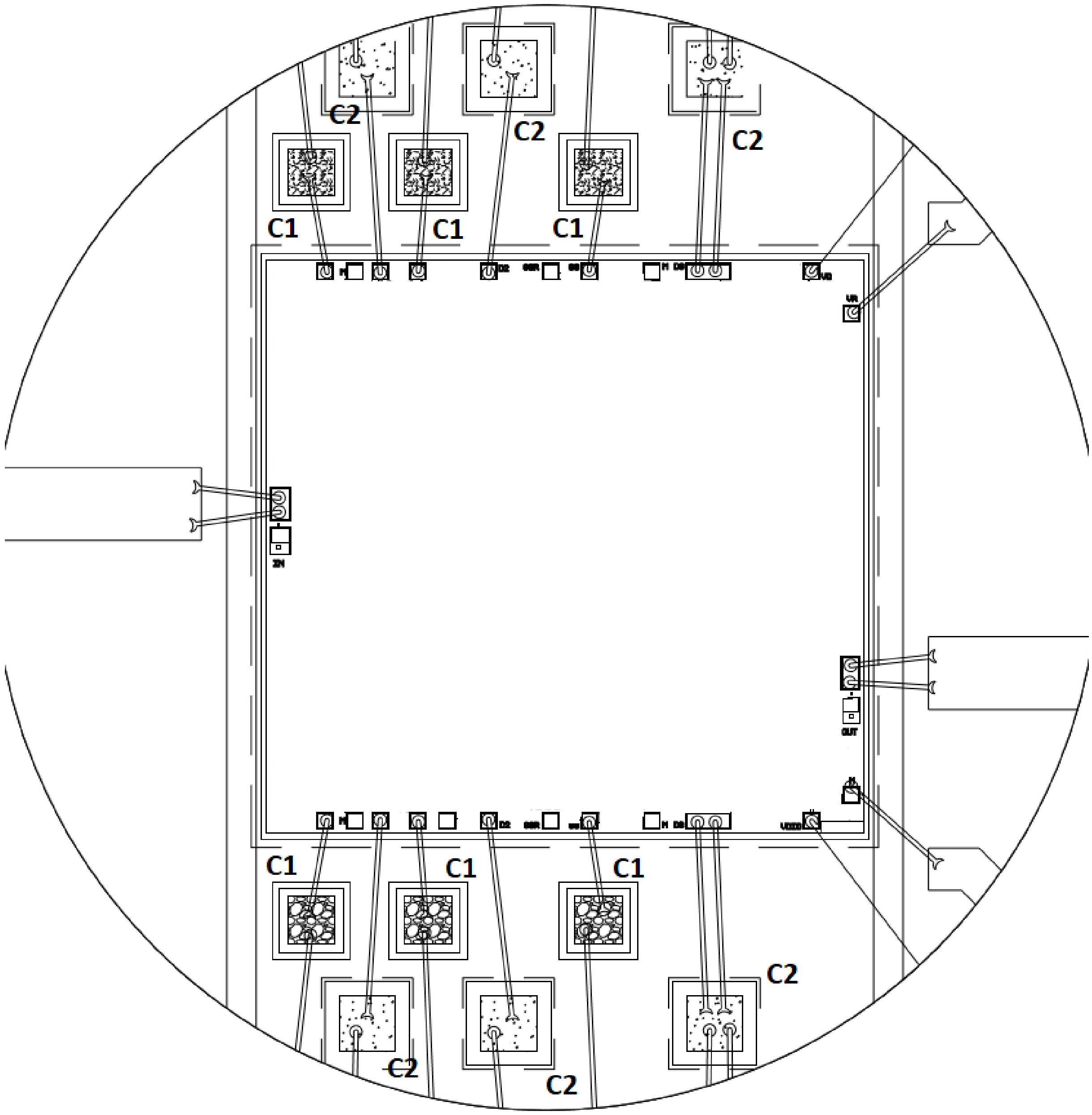
Recommended assembly plan



C1=22pF (on gate access) & C2=120pF (on drain access)

Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

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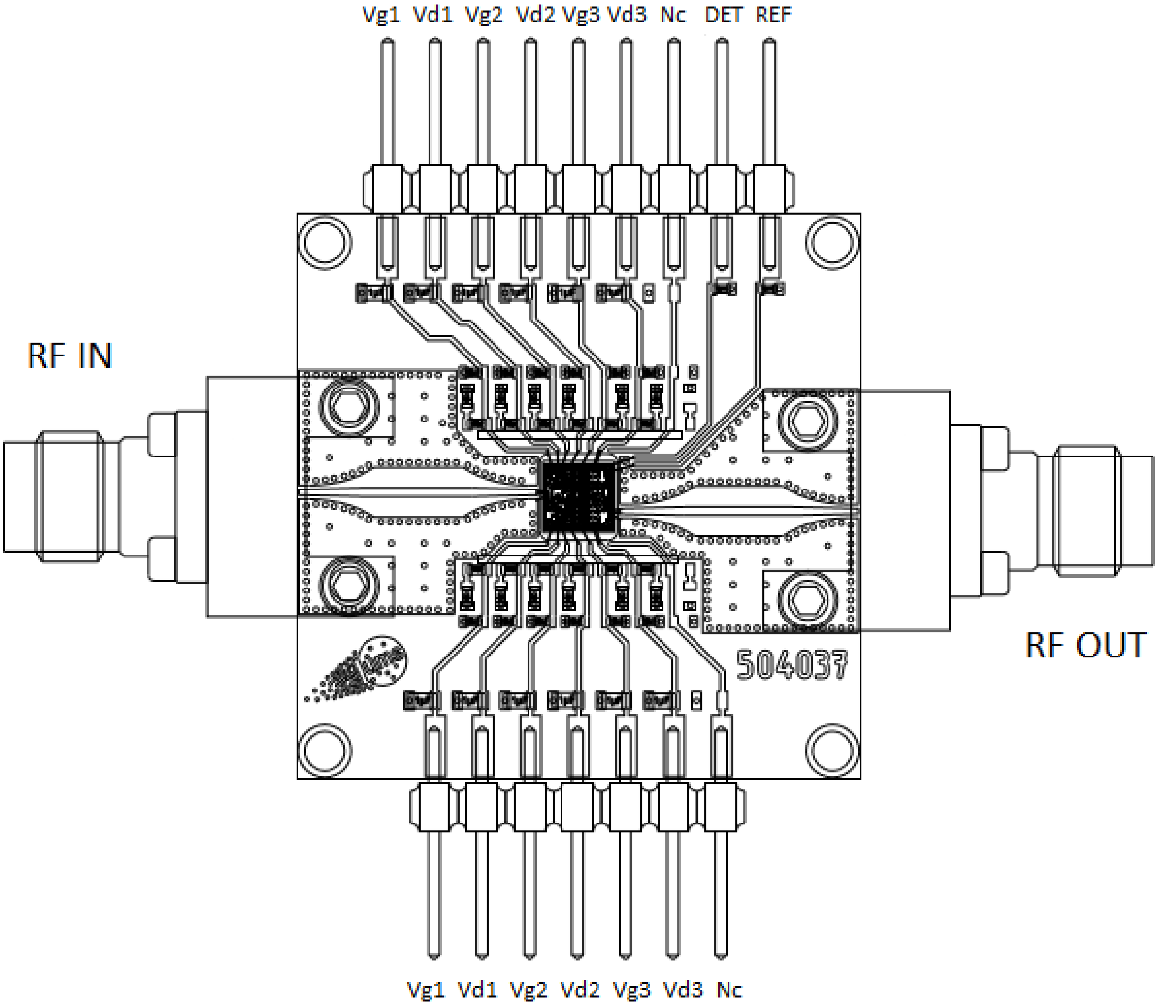
Evaluation mother board

- ■ Compatible with the proposed footprint.
- ■ Based on typically Ro4003C / 8mils or equivalent.
- ■ Using a micro-strip to coplanar transition to access the chip.
- ■ Recommended for the implementation of this product on a module board.
- ■ Decoupling capacitors of 100pF ±10%. 10nF ±10% and 1µF ±10% are recommended for the gate accesses.
- ■ Decoupling capacitors of 100pF ±10%. 10nF ±10% and 1µF ±10% are recommended for the drain accesses.
- ■ A 10KΩ resistor is recommended on VREF & VDET accesses for the detector
- ■ Note: All board measurements are performed using shielded cables. even for DC bias. to ensure safe operation.



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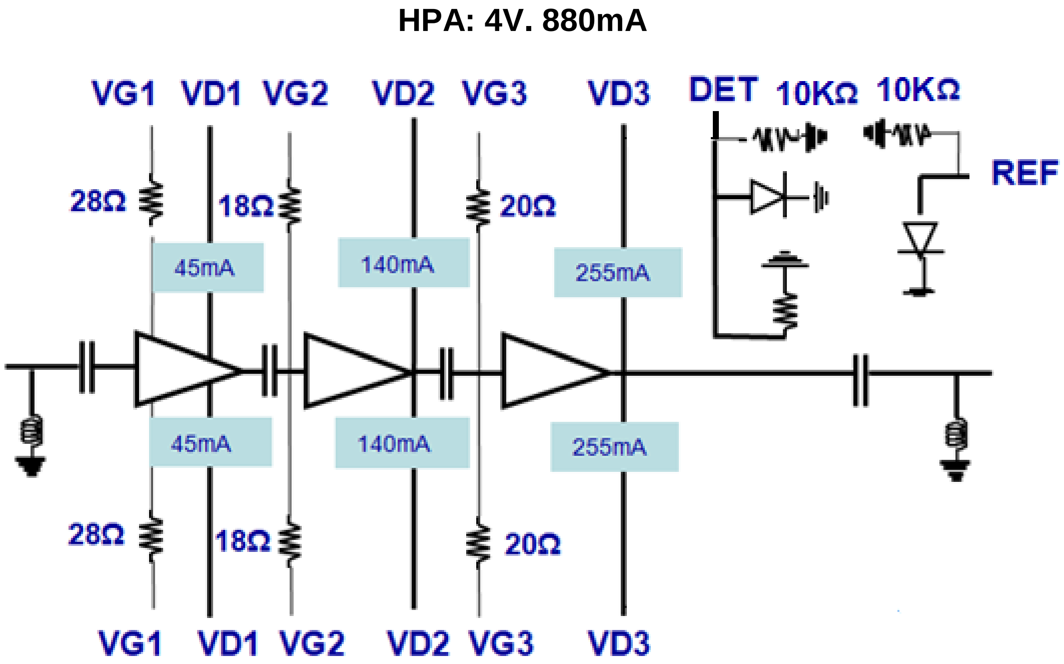
DC Schematic



Biasing procedure

Device Power Up instructions:

1. Ground the device
2. Bias HPA gate voltage at Vg close to Vpinch-off (example: Vg ≈ -2V)
3. Apply Vd quiescent bias voltage (Example: Vd = 4V)
4. Increase slowly Vg up to quiescent bias drain current Id
5. Apply RF input power

Device Power down instructions:

1. Remove RF input power
2. Decrease HPA gate voltage up to Vg -2V
3. Decrease drain voltage up to 0V

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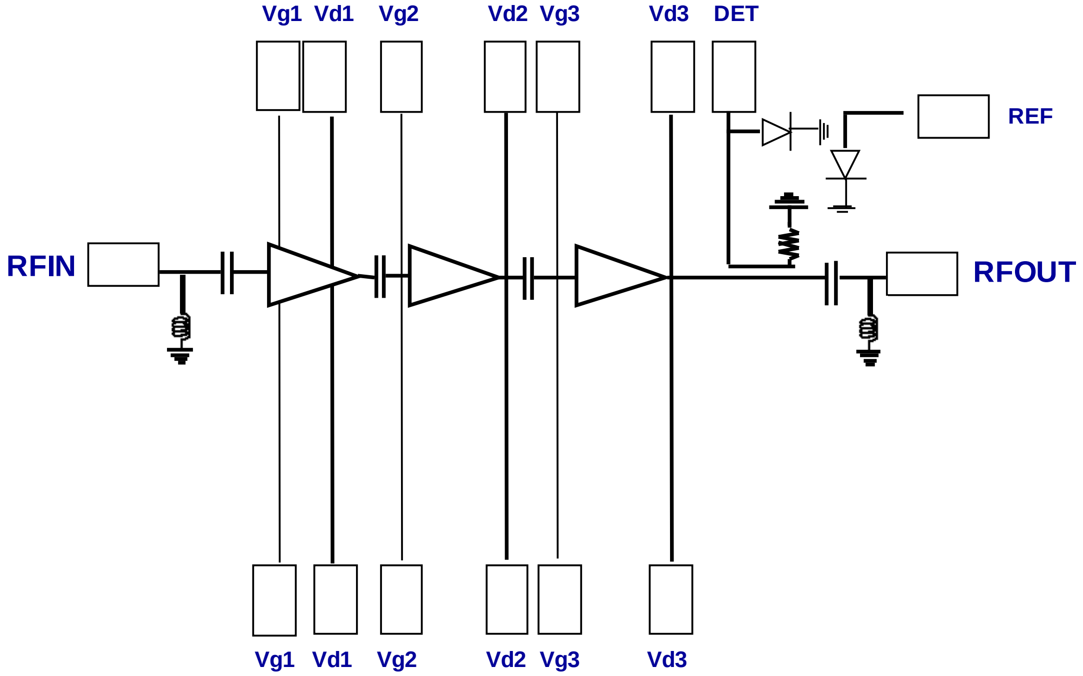
Notes

Due to ESD protection circuits on RF input and output. An external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



The DC connections do not include any decoupling capacitor. Therefore it is mandatory to provide a good external DC decoupling (120pF. 10nF. 1µF) on the PC board as close as possible to the bare die.

A 10KΩ resistor is recommended in parallel to VDET. and VREF accesses

The circuit includes ESD protections on all RF and DC accesses.

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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Ordering Information

Chip form: CHA6551-99F/00

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