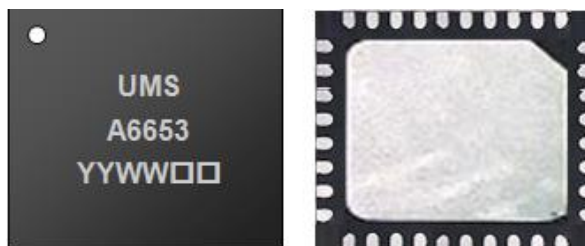


27- 33.5GHz Power Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHA6653-QXG is a four stage monolithic GaAs high power circuit producing 1.8 Watt output power. It is highly linear, with possible gain control and integrates a power detector. ESD protections are included. It is designed for Point To Point Radio. The circuit is manufactured with a pHEMT process, 0.15µm gate length. It is supplied in RoHS compliant SMD package.

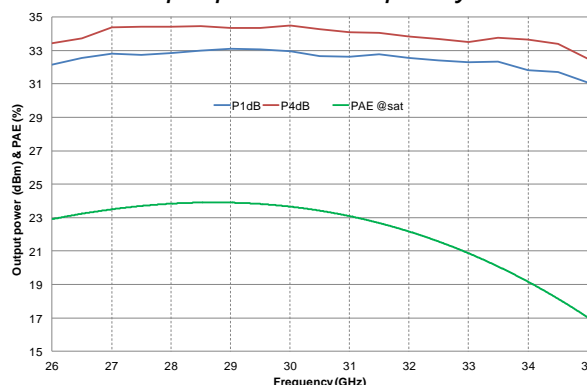


36 lead 6x5 mm QFN package

Main Features

- Broadband performances: 27- 33.5GHz
- 32.5dBm saturated power
- 38dBm OIP3
- 20dB gain
- DC bias: Vd = 6.0Volt @ Id = 0.9A
- QFN 6x5
- MSL3

Output power vs frequency



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27		33.5	GHz
Gain	Linear Gain		20		dB
Psat	Saturated output power		32.5		dBm
OIP3	Output IP3		38		dBm

Electrical Characteristics

Tamb.= +25°C, Vd = +6.0V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	27		33.5	GHz
Gain	Small Signal Gain		20		dB
ΔG	Gain variation in temperature		± 0.03		dB/°C
Psat	Saturated Output Power in 27 - 30GHz Saturated Output Power in 31 - 33.5GHz		33 32.5		dBm
OIP3	Output IP3		38		dBm
PAE	PAE at saturation in 27 - 30GHz PAE at saturation in 31 - 33.5GHz		23 20		%
CG	Gain control range		15		dB
Rlin	Input Return Loss in 27 - 30GHz Input Return Loss in 31 - 33.5GHz		13 10		dB
Rlout	Output Return Loss		12		dB
NF	Noise figure at nominal gain		6		dB
Dr	Detection dynamic range(for output power detection up to Psat)		30		dB
Vdetect	Voltage detection V_{REF} - V_{DET} up to Psat		10 to 2000		mV
Vg	DC gate Voltage		-0.65		V
Idq	Total drain current		0.9		A

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	DC Drain bias voltage without RF	8	V
Id	Drain bias quiescent current	1050	mA
Vg	Gate bias voltage	-2 to 0	V
Pin	Maximum Input Power	+15	dBm
Ta	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above any one of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vd1	8	DC Drain voltage 1 st stage	6.0	V
Vd2	6	DC Drain voltage 2 nd stage	6.0	V
Vd3	4, 23	DC Drain voltage 3 rd stage	6.0	V
Vd4	2, 25	DC Drain voltage 4 th stage	6.0	V
Vg1	19	DC Gate voltage 1 st stage	-0.65	V
Vg2	7, 21	DC Gate voltage 2 nd stage	-0.65	V
Vg3	5, 22	DC Gate voltage 3 rd stage	-0.65	V
Vg4	3, 24	DC Gate voltage 4 th stage	-0.65	V

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).

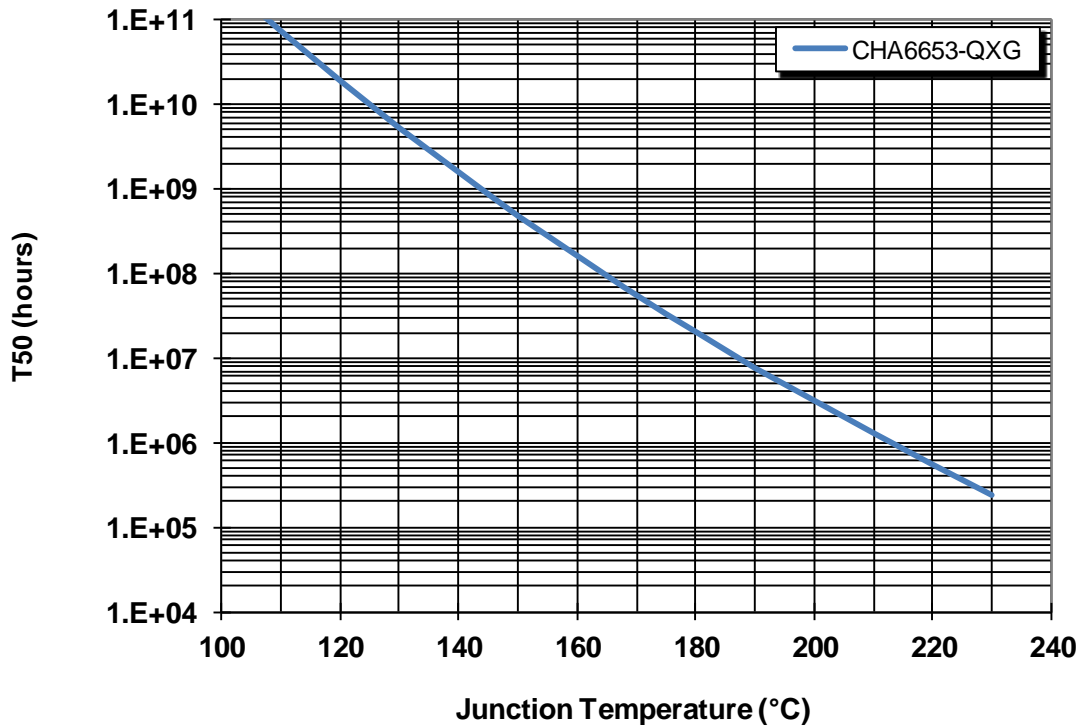
The temperature is monitored at the package back-side interface (Tcase).

The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.

So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R _{TH} (°C/W)	T50 (hours)
R _{TH} ⁽¹⁾ Thermal Resistance (Junction to Case)	Vd= 6V Id= 900mA Pdis= 5.4W	168	15.4	6.8E+07

⁽¹⁾ Assuming 85°C Tcase



Typical Package Sij parameters

Tamb.= +25°C, Vd = +6.0V, Id = 900mA

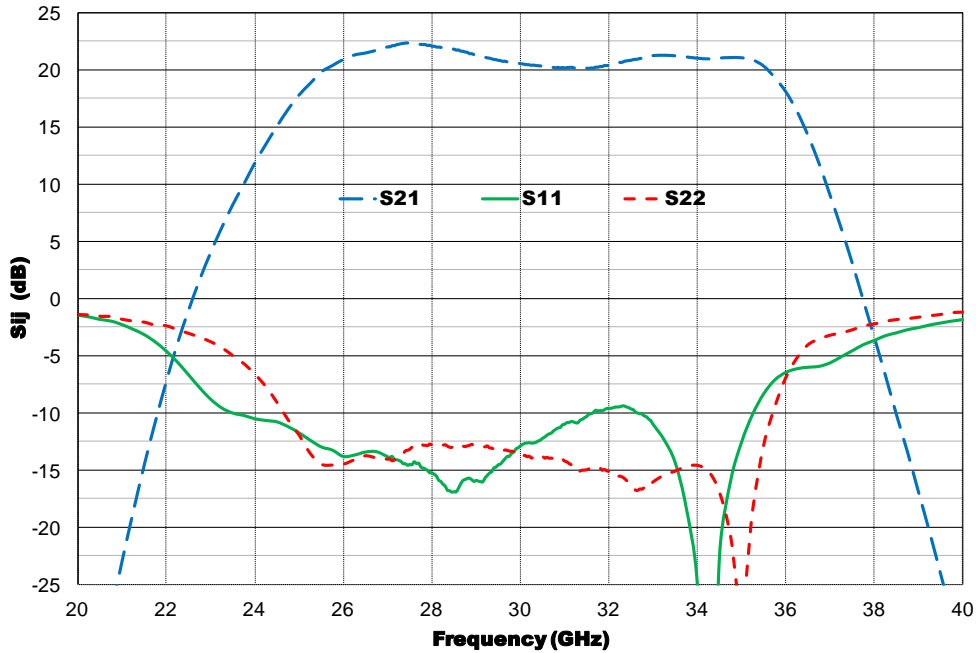
Freq (GHz)	S11 (dB)	PhS11 (°)	S21 (dB)	PhS21 (°)	S12 (dB)	PhS12 (°)	S22 (dB)	PhS22 (°)
1	-0.1	163.8	-72.6	-108.4	-68.7	125.8	-0.1	164.6
2	-0.2	147.7	-71.3	81.2	-65.8	84.6	-0.1	149.6
3	-0.2	132.4	-75.9	170.5	-68.2	83.6	-0.2	134.1
4	-0.2	117.2	-66.0	-1.5	-65.1	58.9	-0.2	118.4
5	-0.2	102.0	-66.2	24.8	-64.0	17.0	-0.2	102.7
6	-0.2	88.0	-60.3	-2.5	-59.1	-6.0	-0.2	86.6
7	-0.2	73.5	-67.5	-11.6	-65.0	-50.2	-0.2	69.8
8	-0.2	60.5	-64.1	-41.2	-62.9	-48.0	-0.3	57.2
9	-0.3	45.3	-63.7	-92.4	-62.8	-78.6	-0.3	40.2
10	-0.3	29.4	-79.0	-93.3	-68.4	-100.5	-0.4	23.4
11	-0.4	12.8	-70.5	-94.8	-64.2	-88.0	-0.4	5.9
12	-0.4	-4.1	-64.4	-148.8	-61.6	-163.8	-0.5	-12.1
13	-0.5	-22.0	-67.8	78.0	-70.3	94.2	-0.7	-31.0
14	-0.5	-40.2	-61.4	-110.8	-59.3	-123.0	-1.3	-55.4
15	-0.6	-59.4	-58.1	129.5	-54.3	125.3	-6.8	-57.2
16	-0.7	-78.7	-65.3	157.3	-60.9	36.3	-1.9	-61.2
17	-0.7	-99.4	-51.4	123.7	-55.1	87.2	-1.3	-85.0
18	-0.9	-121.1	-46.3	66.1	-48.2	46.9	-1.2	-106.4
19	-1.0	-145.4	-50.5	37.6	-49.0	5.8	-1.3	-128.4
20	-1.4	-174.9	-41.6	140.2	-55.5	18.3	-1.4	-153.1
21	-2.2	145.0	-22.9	96.2	-48.9	-2.7	-1.8	178.2
22	-4.6	84.3	-7.2	6.1	-46.6	-48.1	-2.4	147.2
23	-8.8	-10.5	4.1	-108.2	-50.0	-34.6	-3.8	109.6
24	-10.5	-117.5	11.9	135.5	-46.0	-50.9	-6.6	68.9
25	-11.7	147.3	17.8	16.2	-44.2	-66.9	-11.9	39.4
26	-13.8	45.3	20.9	-104.9	-43.5	-86.9	-14.5	42.1
27	-13.8	-31.1	22.0	143.4	-43.6	-123.4	-14.0	22.8
28	-15.2	-63.9	22.1	35.2	-44.9	-124.2	-12.8	-6.6
29	-15.9	-63.6	21.4	-64.1	-44.0	-150.8	-12.8	-45.7
30	-12.8	-68.7	20.6	-156.3	-44.9	-133.7	-13.6	-90.0
31	-11.0	-89.0	20.2	113.9	-45.0	-135.2	-14.2	-135.3
32	-9.6	-121.1	20.5	23.7	-42.5	-145.9	-15.1	-173.5
33	-11.0	-173.5	21.3	-75.6	-40.7	-169.6	-16.0	165.2
34	-25.0	120.5	21.0	176.6	-41.2	179.9	-14.6	136.8
35	-12.5	-117.1	21.1	59.3	-37.7	173.4	-27.1	149.4
36	-6.4	172.2	18.1	-84.0	-34.2	145.8	-6.9	171.1
37	-5.6	130.0	9.1	134.9	-35.0	98.9	-3.2	117.4
38	-3.6	99.1	-3.4	23.3	-36.7	75.3	-2.2	86.2
39	-2.5	72.3	-16.9	-59.6	-39.2	41.8	-1.6	59.2
40	-1.8	51.2	-32.0	-132.6	-42.9	43.7	-1.2	36.0

Typical Board Measurements

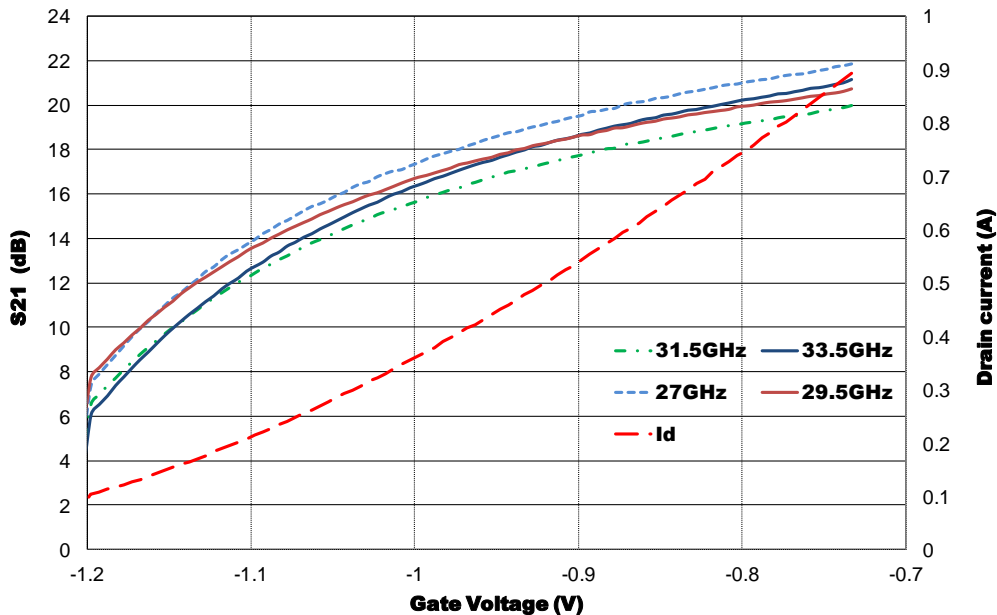
Tamb.= +25°C, Vd = +6.0V, Id = 900mA

Measurement performed in the access plans of the QFN, using the proposed land pattern & board, as defined in paragraph "Evaluation mother board"

Gain & Return Loss versus Frequency

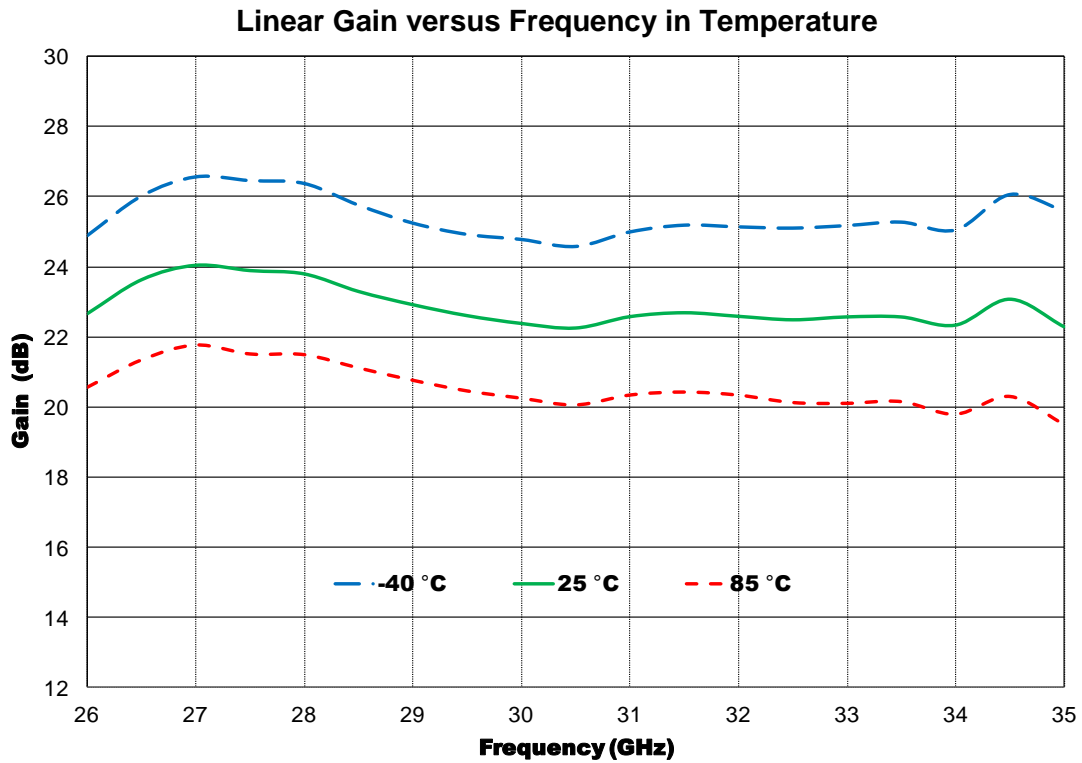
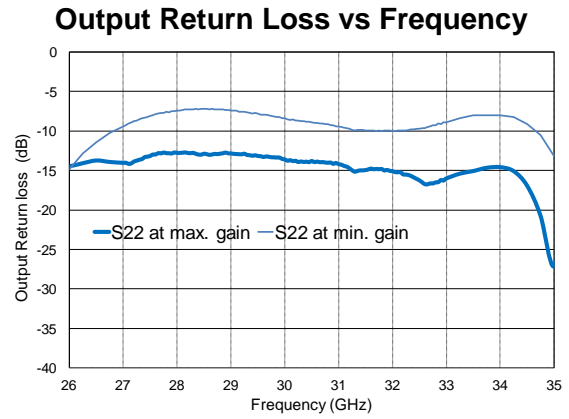
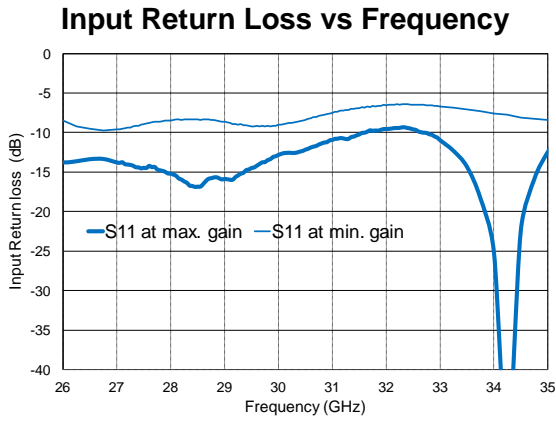


Gain control & current versus Gate Voltage



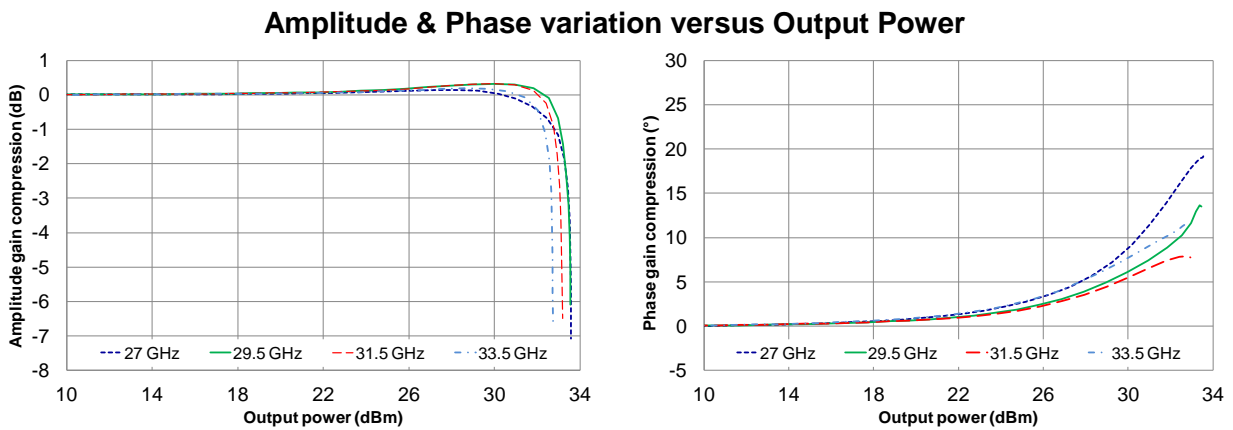
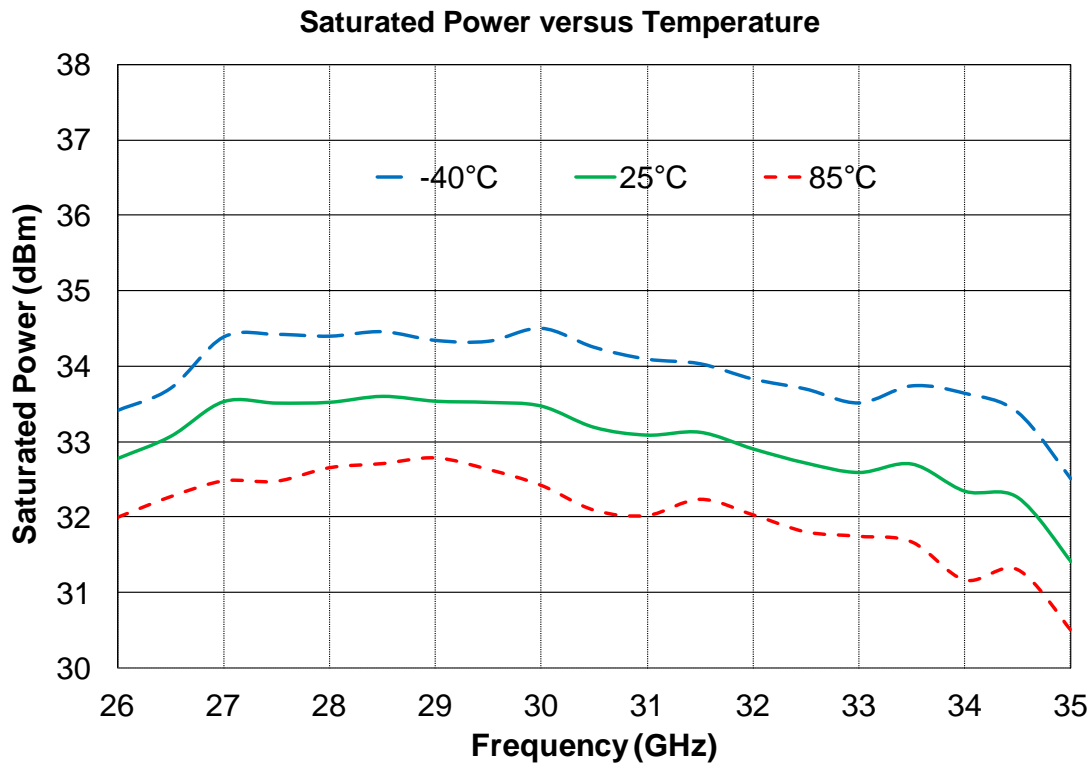
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 900mA



Typical Board Measurements

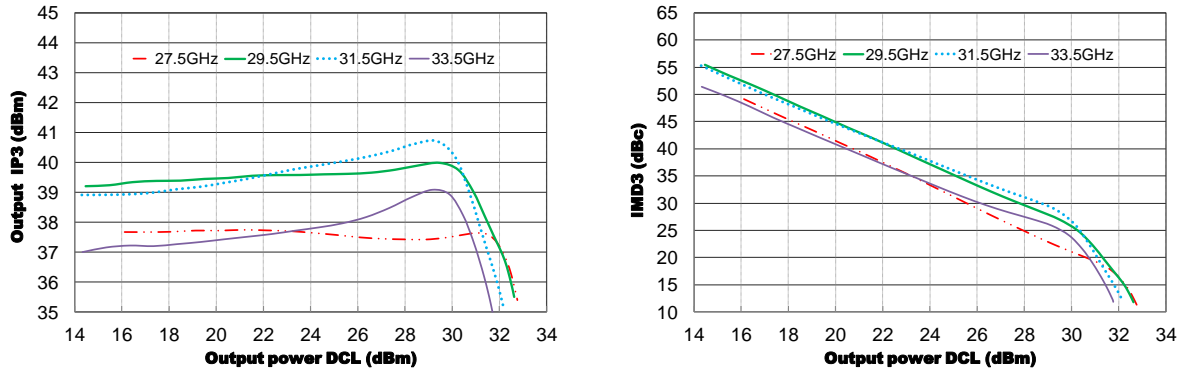
Tamb.= +25°C, Vd = +6.0V, Id = 900mA



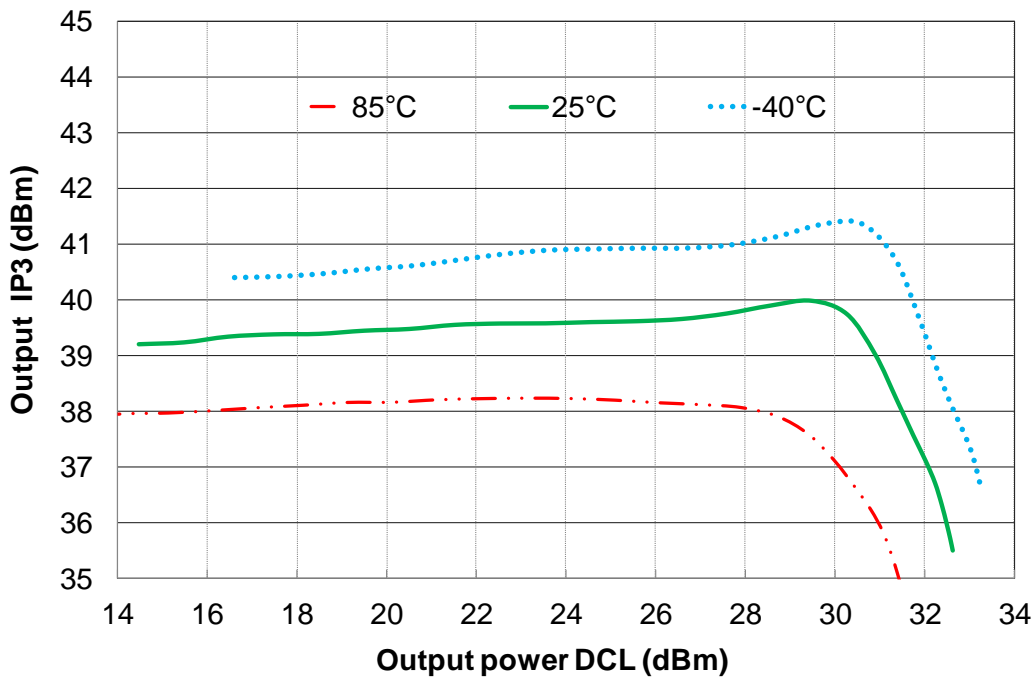
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 900mA

Output IP3 & IMD3 versus Output Power

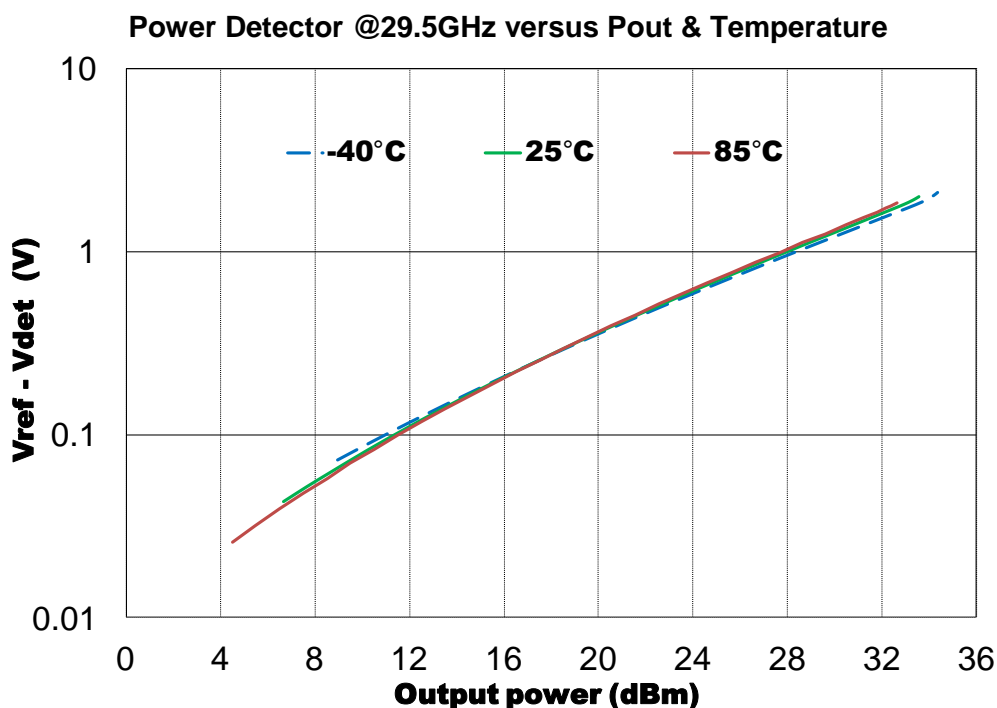
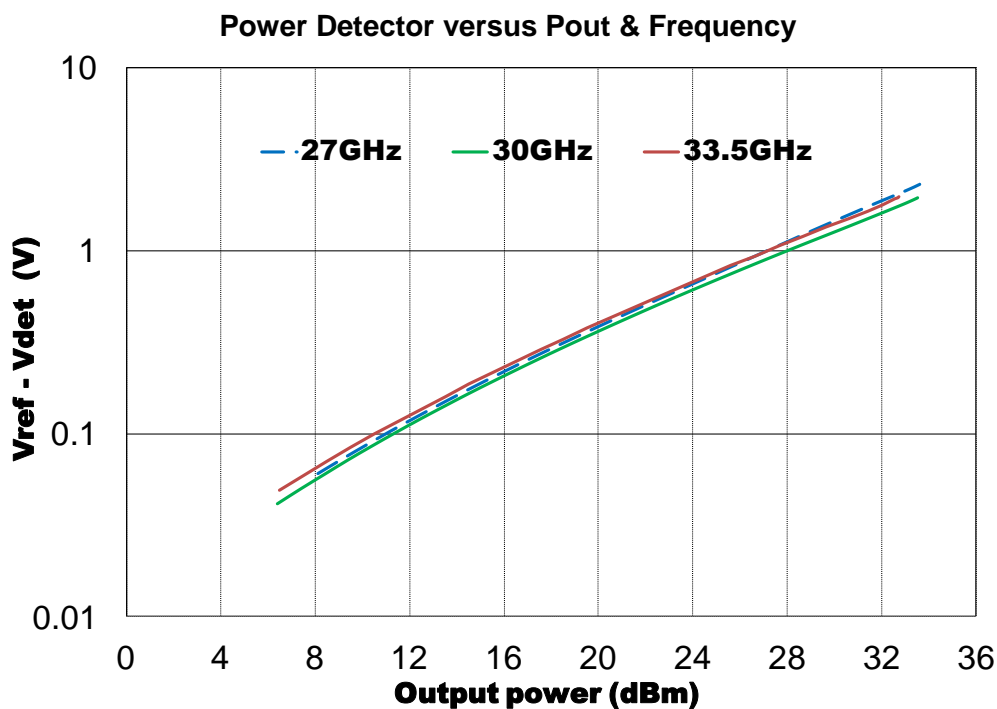


Output IP3 with temperature at 29.5GHz

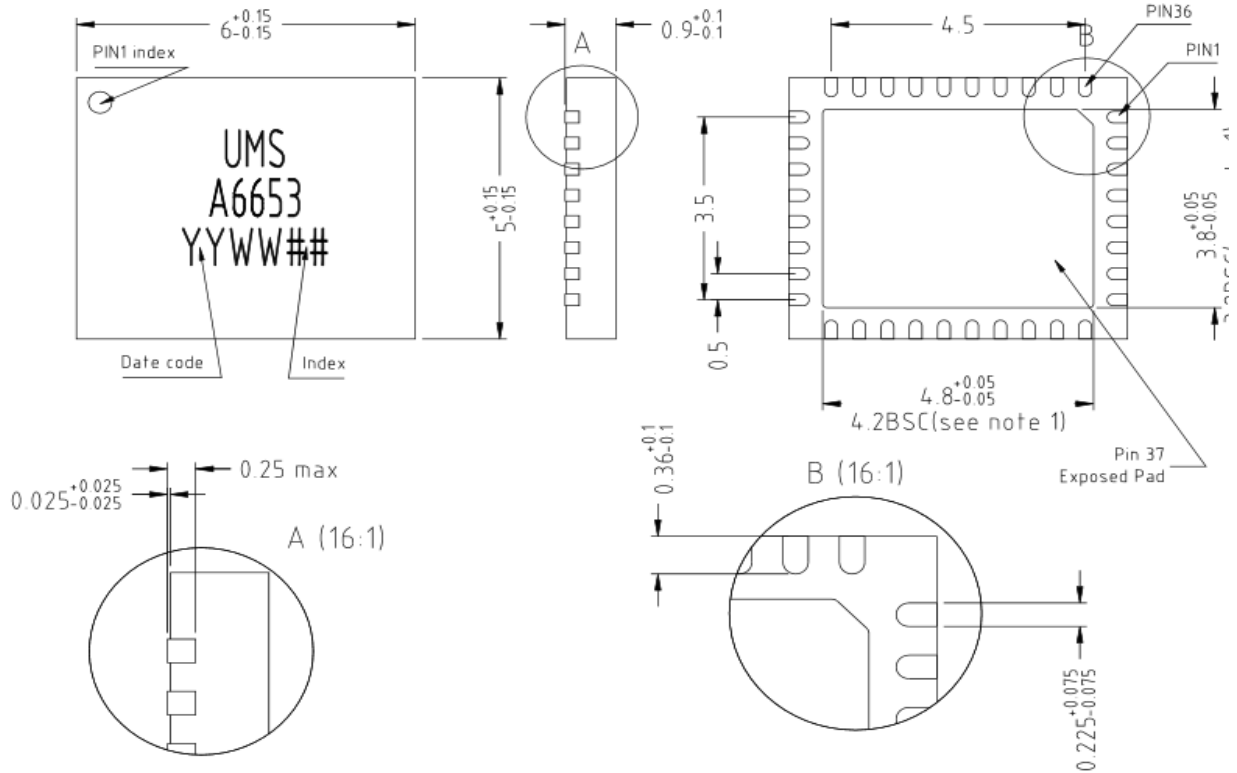


Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 900mA



Package outline (1)



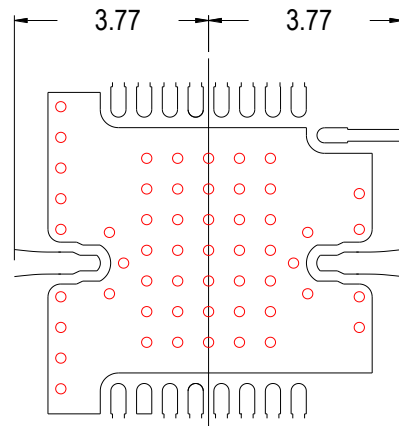
Matte tin, Lead Free (Green)	1- DET	13- Gnd ⁽²⁾	25- Vd4
Units : mm	2- Vd4	14- RF in	26- NC
From the standard : JEDEC MO-220 (VGGD)	3- Vg4	15- Gnd ⁽²⁾	27- Gnd ⁽²⁾
37- GND	4- Vd3	16- NC	28- NC
	5- Vg3	17- NC	29- NC
	6- Vd2	18- NC	30- Gnd ⁽²⁾
	7- Vg2	19- Vg1	31- RF out
	8- Vd1	20- NC	32- Gnd ⁽²⁾
	9- NC	21- Vg2	33- NC
	10- NC	22- Vg3	34- NC
	11- NC	23- Vd3	35- NC
	12- NC	24- Vg4	36- REF

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<https://www.ums-rf.com>) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.77mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation motherboard".



ESD sensitivity

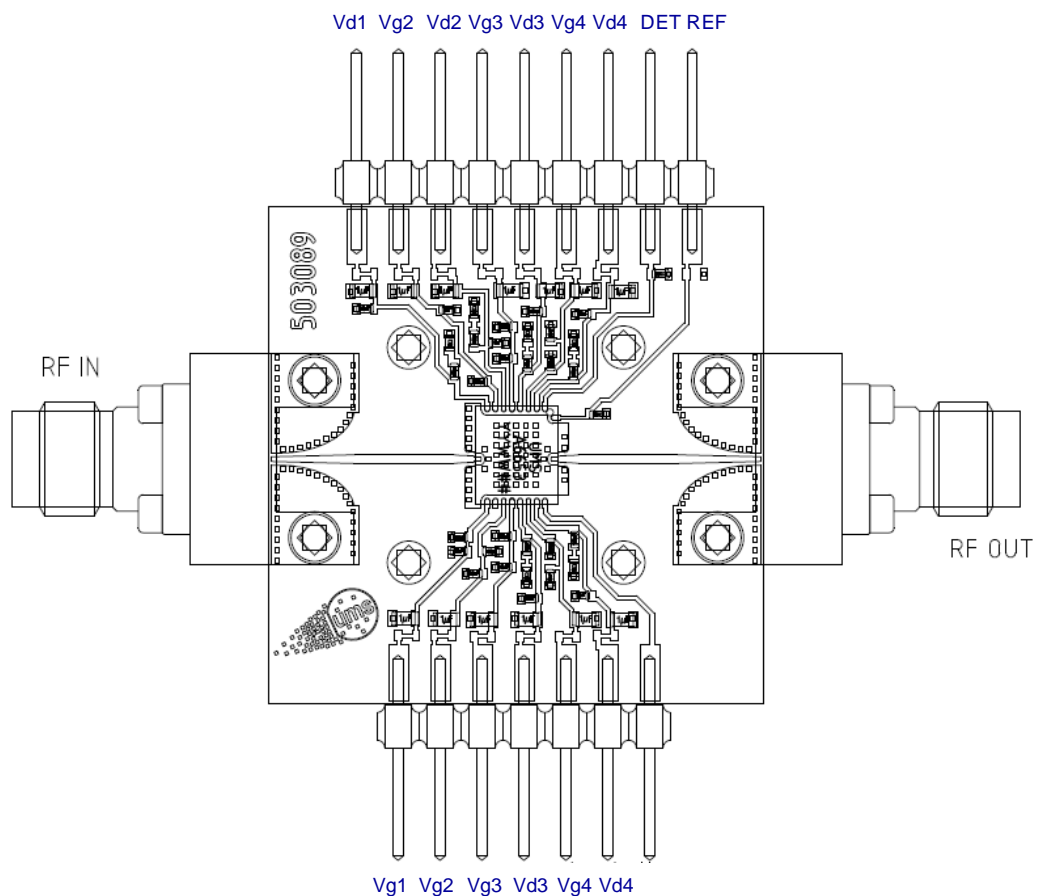
Standard	Value
MIL-STD-1686C	HBM Class 1 (<2000V)

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL3

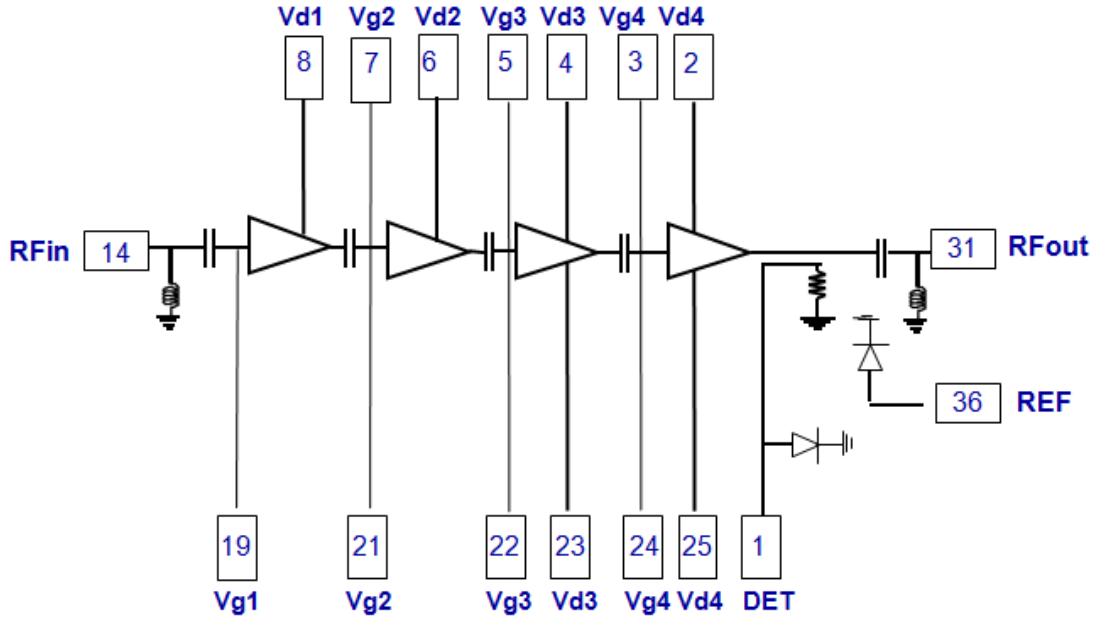
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4350B / 10mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF \pm 5%, 10nF \pm 10% and 1 μ F \pm 10% are recommended for DC accesses.
- A 10K Ω resistor is recommended on VREF & VDET accesses for the detector
- See application note AN0017 for details.



Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage potentially present on the RF accesses.



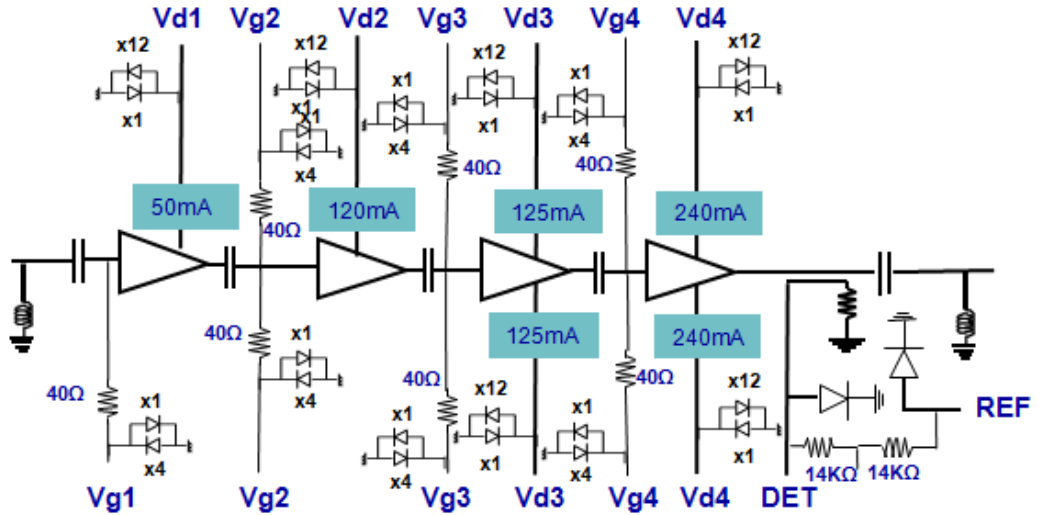
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package (See paragraph “Evaluation mother board”).

A 10KΩ resistor is recommended in parallel to VDET, and VREF accesses.

The circuit includes ESD protections on all RF and DC leads

DC Schematic

6V, 900mA



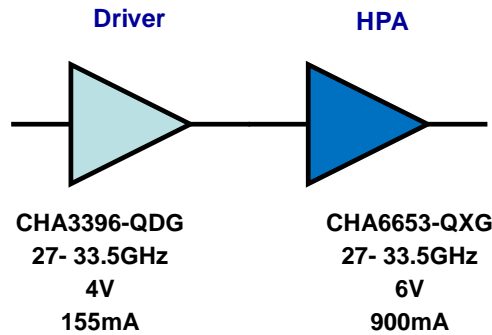
Recommended UMS Power chain

The CHA6653-QXG is recommended with the CHA3396-QDG as driver.

Total Gain: 44dB

Gain control: 30dB with the both amplifiers.

For more information about the CHA3396-QDG, see our web site www.ums-gaas.com



Recommended package footprint

Refer to the application note AN0017 available at <https://www.ums-rf.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 6x5 package:

CHA6653-QXG/XY

Stick: XY = 20

Tape & reel: XY = 21

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