

17-24GHz Integrated Down Converter

GaAs Monolithic Microwave IC in SMD leadless package

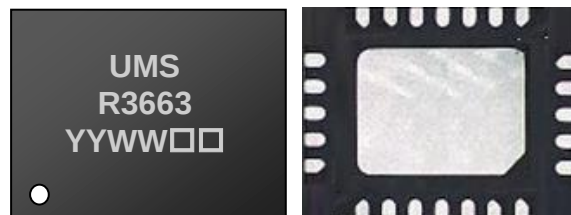
Description

The CHR3663-QEG is a multifunction part, which integrates a balanced cold FET mixer, a multiplier by two, and a RF LNA including gain control.

It is designed for a wide range of applications, typically commercial communication systems and ISM.

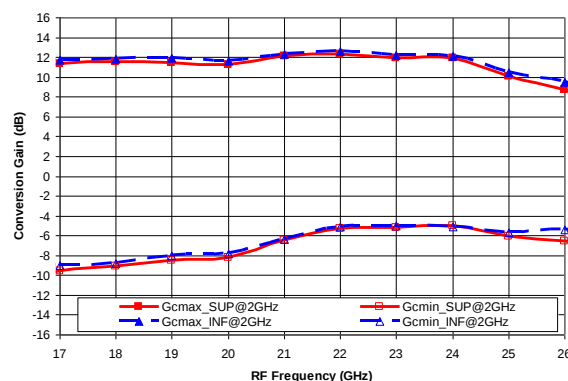
The circuit is manufactured with a robust high volume pHEMT process, 0.25μm gate length.

It is available in lead-free SMD package.



Main Features

- Broadband RF performance 17-24GHz
- 11dB conversion gain
- 15dBc Image Rejection
- 3dBm Input IP3
- 15dB Gain control
- 24LQFN4x5
- MSL1



Main Characteristics

Tamb = +25°C, Vd = 4.5V

Symbol	Parameter	Min	Typ	Max	Unit
F _{RF}	RF frequency range	17.0		24.0	GHz
F _{LO}	LO frequency range	7.0		14.0	GHz
F _{IF}	IF frequency range	DC		3.5	GHz
G _c	Conversion gain		11		dB

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

Electrical Characteristics

T_{amb} = +25°C, V_D = V_{DL} = 4.5V

Symbol	Parameter	Min	Typ	Max	Unit
F _{RF}	RF frequency range	17.0		24.0	GHz
F _{LO}	LO frequency range	7.0		14.0	GHz
F _{IF}	IF frequency range	DC		3.5	GHz
G _c	Conversion gain@ min. attenuation (1)	8.5	11.0		dB
ΔG	Gain control range		15		dB
NF	Noise Figure@ min. attenuation, for IF>0.1GHz		3.5	4.5	dB
Im_rej	Image rejection (1)		15		dBc
P _{LO}	LO Input power		0		dBm
IIP3	Input IP3@ min. att.	0	3		dBm
2LO/RF	2LO leakage at RF port @ max. gain		-40		dBm
V _D , V _{DL}	DC drain voltage		4.5		V
I _d	Drain current		380		mA
V _{GL}	LNA DC gate voltage		-0.4		V
GC2, GC3	Gain control DC voltage	-2.0		+0,6	V
V _{GM}	Mixer DC gate voltage		-0.7		V

These values are representative of onboard measurements as defined on the drawing at paragraph "Evaluation mother board".

(1) An external combiner 90° is required on I / Q.

Note: I_d not affected by GC2, GC3.

Absolute Maximum Ratings ⁽¹⁾T_{amb} = +25°C

Symbol	Parameter	Values	Unit
V _d	Maximum drain bias voltage	5	V
I _d	Maximum drain bias current	450	mA
V _{GL} , V _{GM}	LNA, mixer DC gate voltage	-2.0 to +0.4	V
GC1, 2	Gain control voltage	-2.5 to + 0.8	V
P _{RF}	Maximum peak input power overdrive	10	dBm
P _{LO}	Maximum LO input power	10	dBm
T _{ch}	Maximum channel temperature	175	°C
T _a	Operating temperature range	-40 to +85	°C
T _{stg}	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (T_{case}) as shown below. The system maximum temperature must be adjusted in order to guarantee that T_{case} remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

A derating must be applied on the dissipated power if the T_{case} temperature can not be maintained below than the maximum temperature specified in order to guarantee the nominal device life time (MTTF) (see the curve $P_{diss. Max}$).

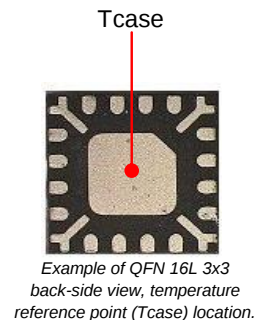
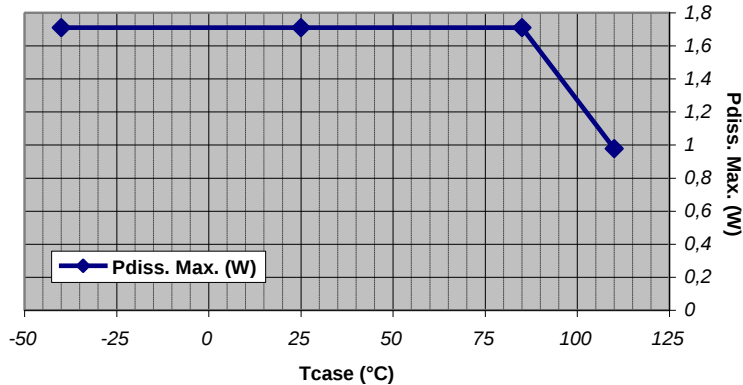
DEVICE THERMAL SPECIFICATION : CHR3663-QEG

Recommended max. junction temperature (T_j max)	:	143 °C
Junction temperature absolute maximum rating	:	175 °C
Max. continuous dissipated power @ $T_{case} = 85$ °C	:	1,71 W
=> P_{diss} derating above $T_{case}^{(1)} = 85$ °C	:	29 mW/°C
Junction-Case thermal resistance ($R_{th J-C}^{(2)}$)	:	<34 °C/W
Min. package back side operating temperature ⁽³⁾	:	-40 °C
Max. package back side operating temperature ⁽³⁾	:	85 °C
Min. storage temperature	:	-55 °C
Max. storage temperature	:	125 °C

(1) Derating at junction temperature constant = T_j max

(2) $R_{th J-C}$ is calculated for a worst case where the **hotter junction** of the MMIC is considered.

(3) T_{case} = Package back side temperature measured under the die-attach-pad (see the drawing below).



5.6

Typical Measured Performances

$T_{amb} = +25^{\circ}\text{C}$, $V_D = V_{DL} = 4.5\text{V}$, $V_{GL} = -0.4\text{V}$, $V_{GM} = -0.7\text{V}$, $P_{LO} = 0\text{dBm}$

These values are representative of onboard measurements (on connector access planes) as defined on the drawing 97625 page 16. The board losses are estimated from 1.5 to 2.0dB in the frequency range.

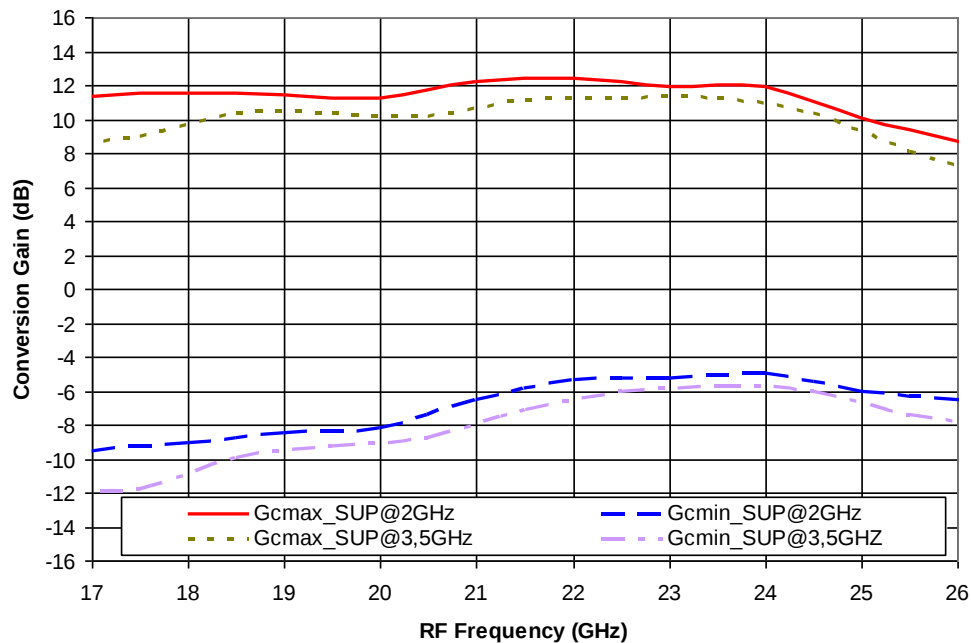


Figure 1: Conversion Gain in Supradyn Mode versus Frequency
 $F_{RF} = 2x F_{LO} + F_{IF}$, $F_{IF} = 2.0 \text{ \& } 3.5\text{GHz}$, $GC2 = GC3 = -1.5 \text{ \& } 0.5\text{V}$

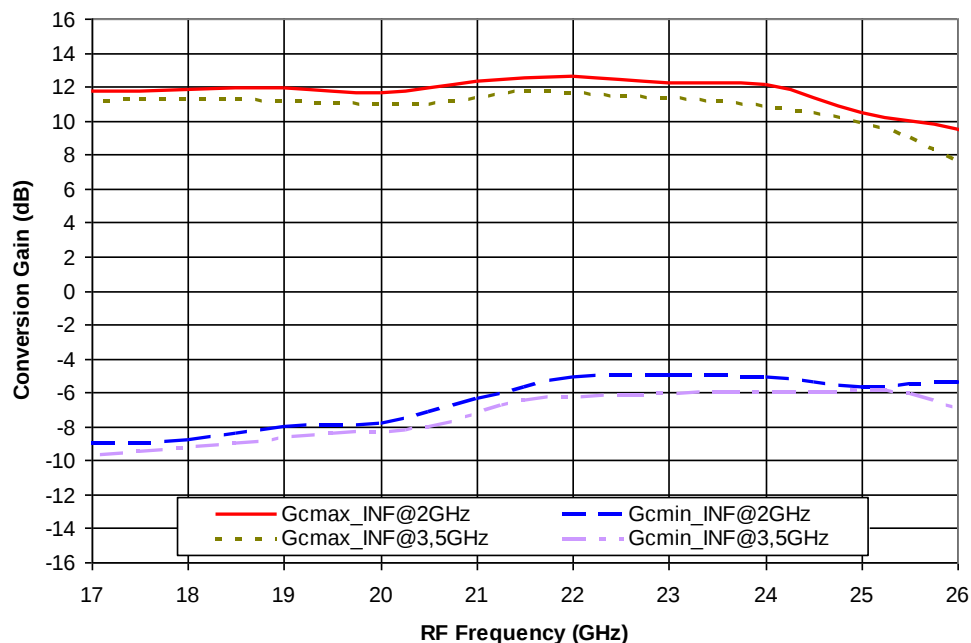


Figure 2: Conversion Gain in Infradyne Mode versus Frequency
 $F_{RF} = 2x F_{LO} - F_{IF}$, $F_{IF} = 2.0 \text{ \& } 3.5\text{GHz}$, $GC2 = GC3 = -1.5 \text{ \& } 0.5\text{V}$

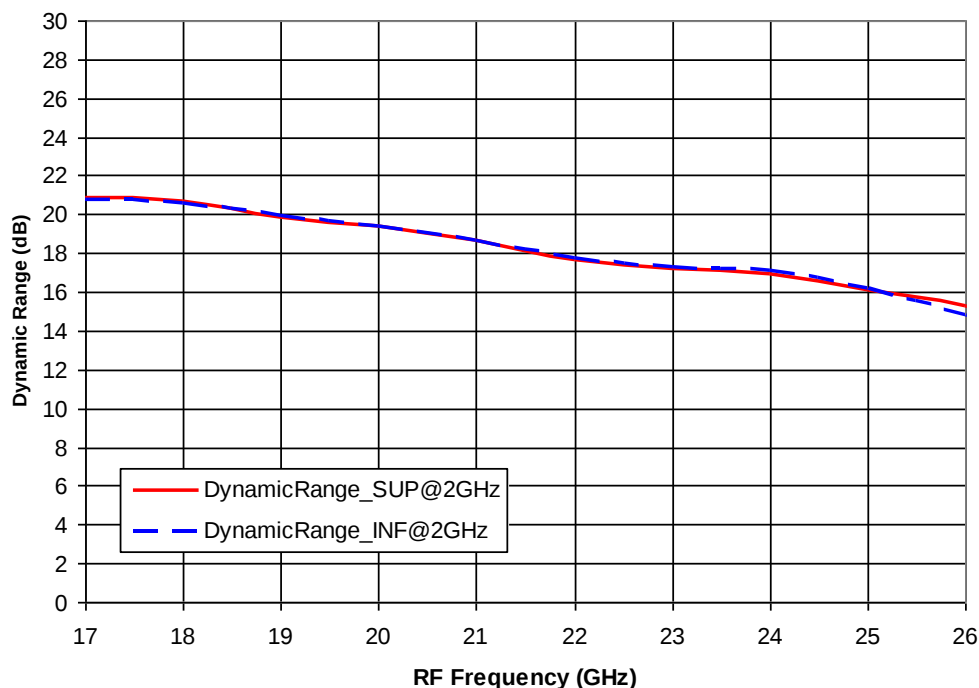


Figure 3: Dynamic Range (Gcmax – Gcmin) versus Frequency
 $F_{RF} = 2 \times F_{LO} - F_{IF}$ & $F_{RF} = 2 \times F_{LO} + F_{IF}$, $F_{IF} = 2.0\text{GHz}$

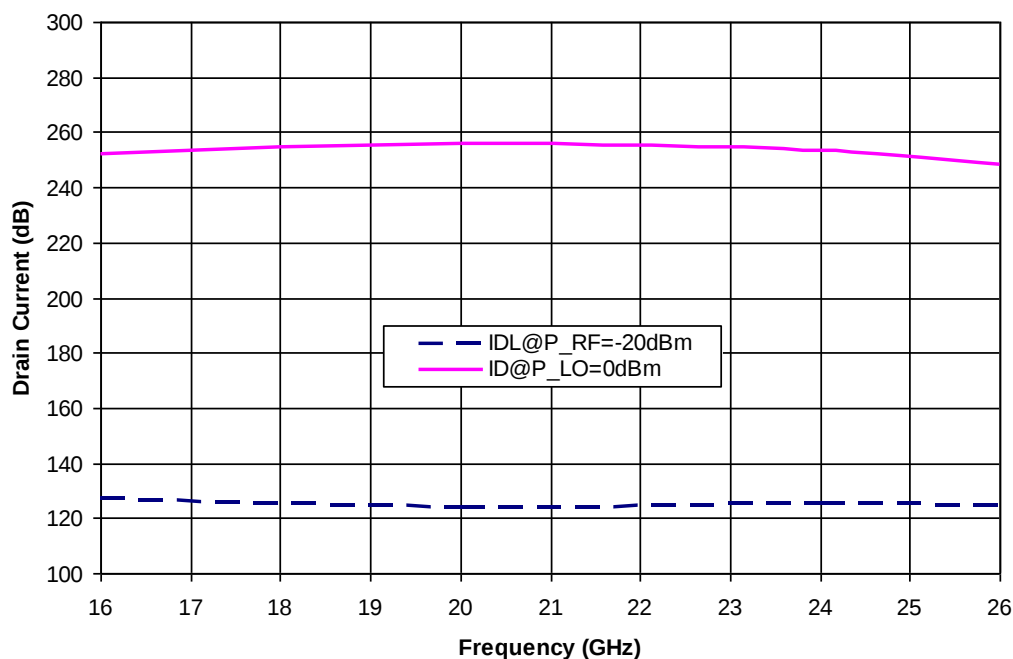


Figure 4: Drain Currents versus Frequency
 $F_{RF} = 2 \times F_{LO} - F_{IF}$, $Freq_{IF} = 2.0\text{GHz}$, $GC2 = GC3 = -1.5\text{V}$

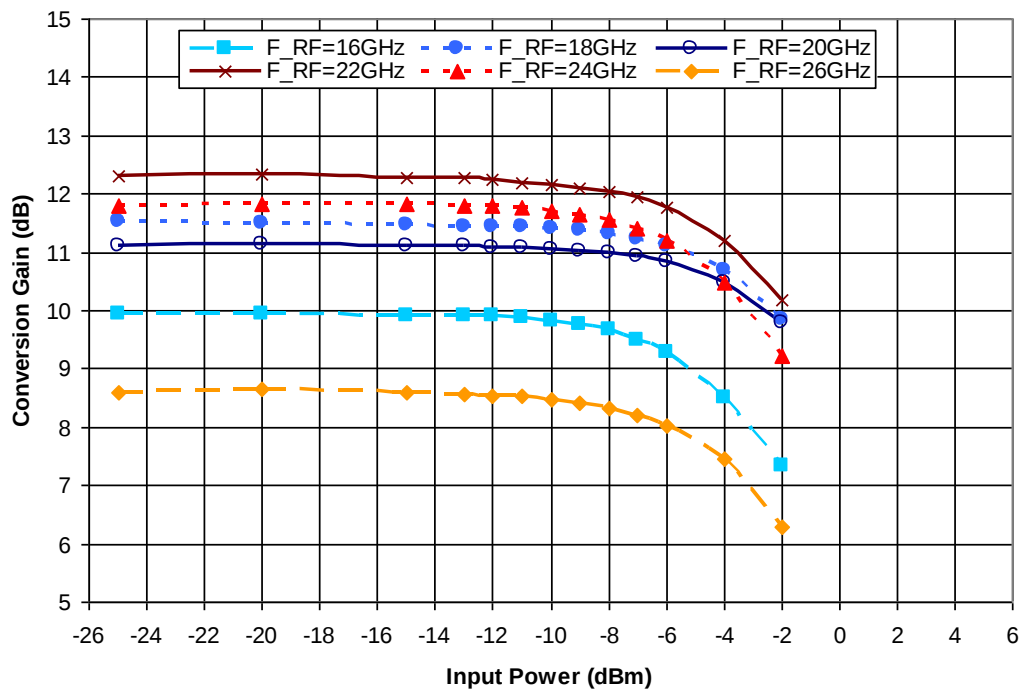


Figure 5 : Conversion Gain versus RF Power & Frequency

$F_{RF} = 2 \times F_{LO} + F_{IF}$, $F_{IF} = 2.0\text{GHz}$, $GC2 = GC3 = -1.5\text{V}$

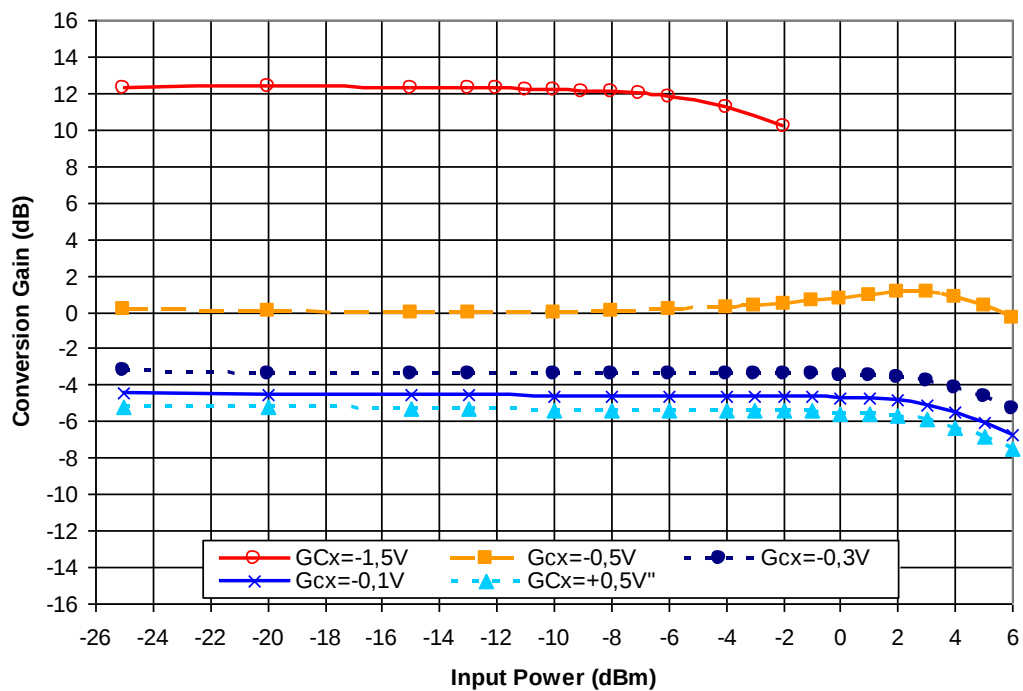


Figure 6: Conversion Gain versus RF Power & Gain control

$F_{RF} = 2 \times F_{LO} + F_{IF}$, $F_{RF} = 20\text{GHz}$, $F_{IF} = 2.0\text{GHz}$

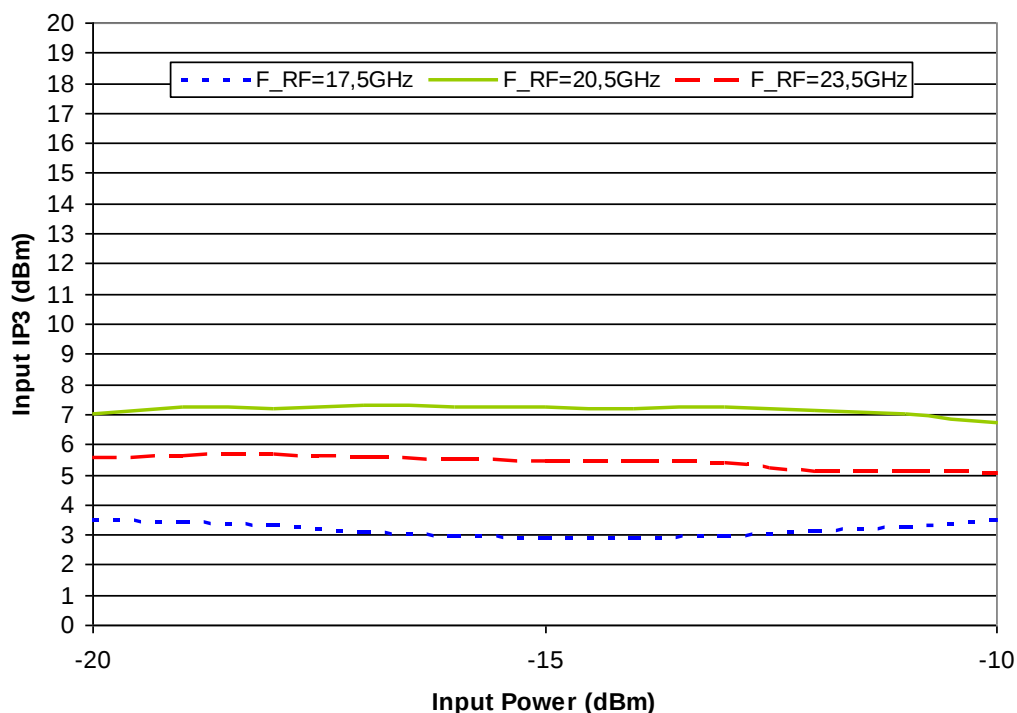


Figure 7: Input IP3 versus RF Frequency & RF Power (Double Carrier)

$F_{RF} = 2 \times F_{LO} - F_{IF}$, $F_{IF} = 3.5\text{GHz}$, $GC2 = GC3 = -1.5\text{V}$

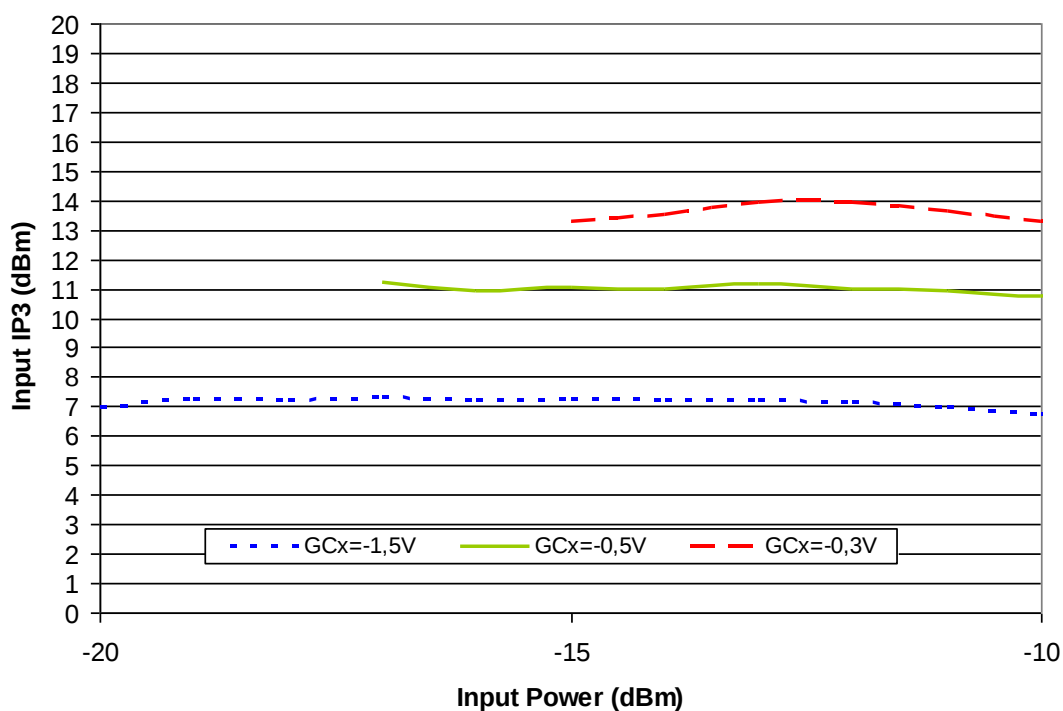


Figure 8: Input IP3 versus Gain Control & RF Power (Double Carrier)

$F_{RF} = 2 \times F_{LO} - F_{IF}$, $F_{RF} = 20.5\text{GHz}$, $F_{IF} = 3.5\text{GHz}$

Temperature Measurements

$T = [-40, +25, 85] ^\circ\text{C}$, $V_D = V_{DL} = 4.5\text{V}$, $V_{GL} = -0.4\text{V}$, $V_{GM} = -0.7\text{V}$, $P_{LO} = 0\text{dBm}$

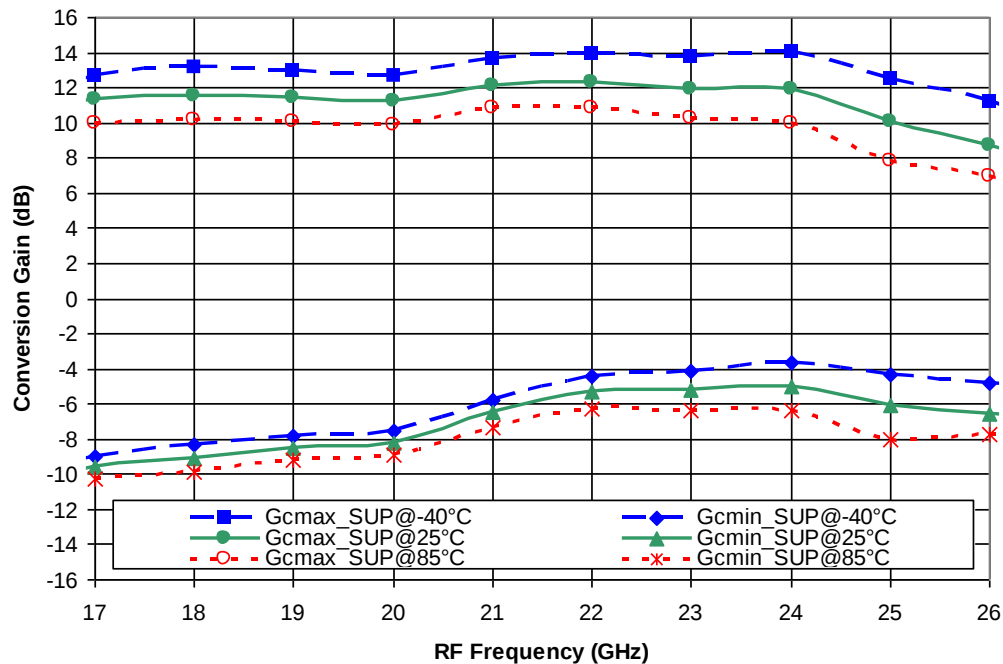


Figure 9: Conversion Gain in Supradyn Mode versus Temperature & Frequency

$F_{RF} = 2 \times F_{LO} + F_{IF}$, $F_{IF} = 2.0\text{GHz}$, $GC2 = GC3 = -1.5 \text{ \& } 0.5\text{V}$

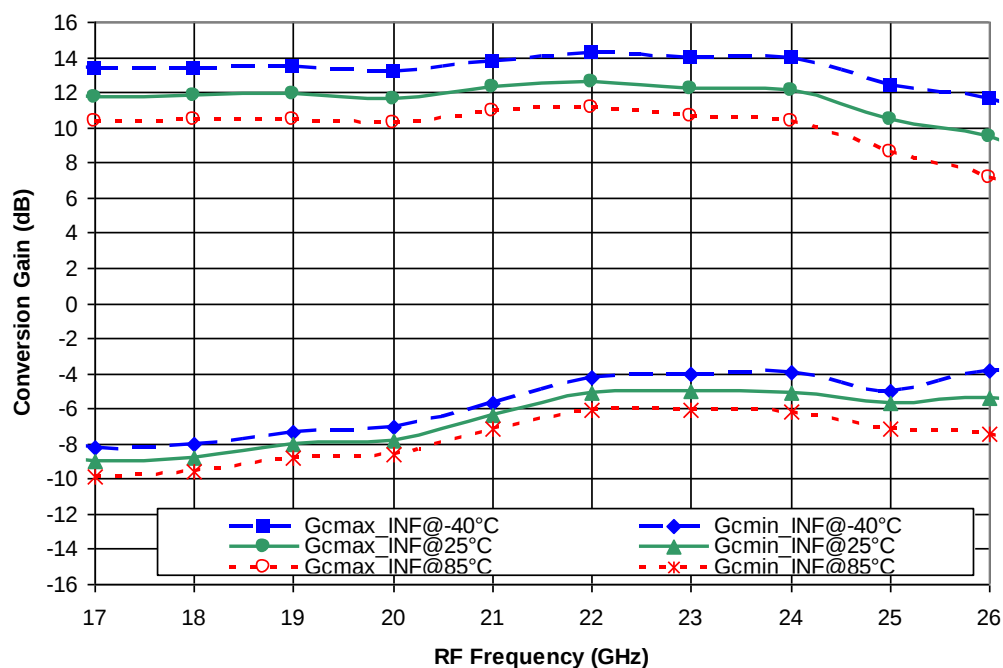


Figure 10: Conversion Gain in Infradyne Mode versus Temperature & Frequency

$F_{RF} = 2 \times F_{LO} - F_{IF}$, $F_{IF} = 2.0\text{GHz}$, $GC2 = GC3 = -1.5 \text{ \& } 0.5\text{V}$

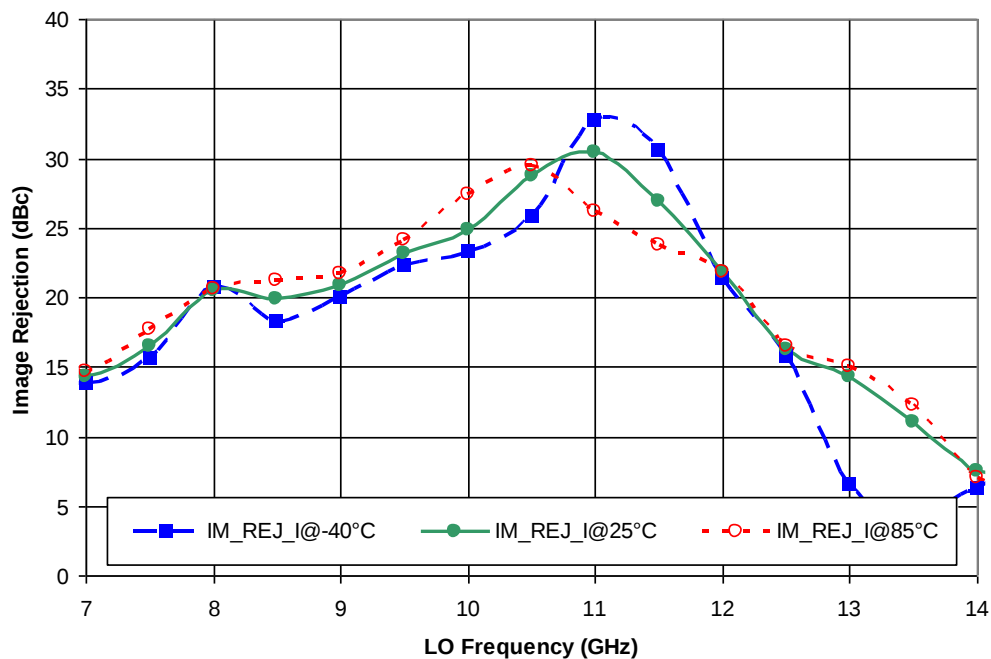


Figure 11: Image Rejection on Output I
 $F_{IF} = 2.0\text{GHz}$, $GC2 = GC3 = -1.5\text{V}$

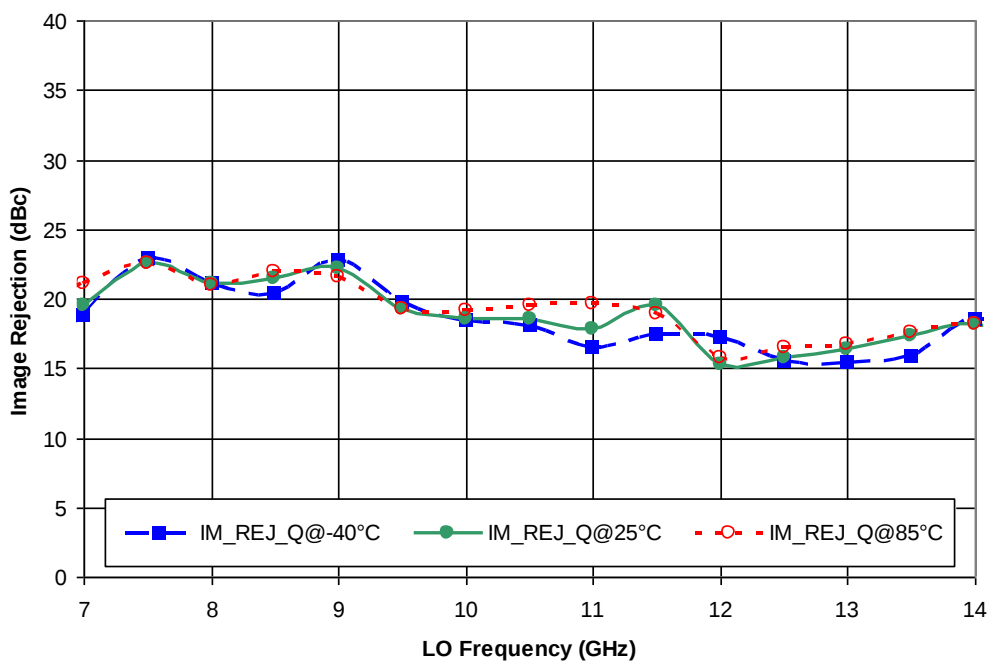


Figure 12: Image Rejection on Output Q
 $F_{IF} = 2.0\text{GHz}$, $GC2 = GC3 = -1.5\text{V}$

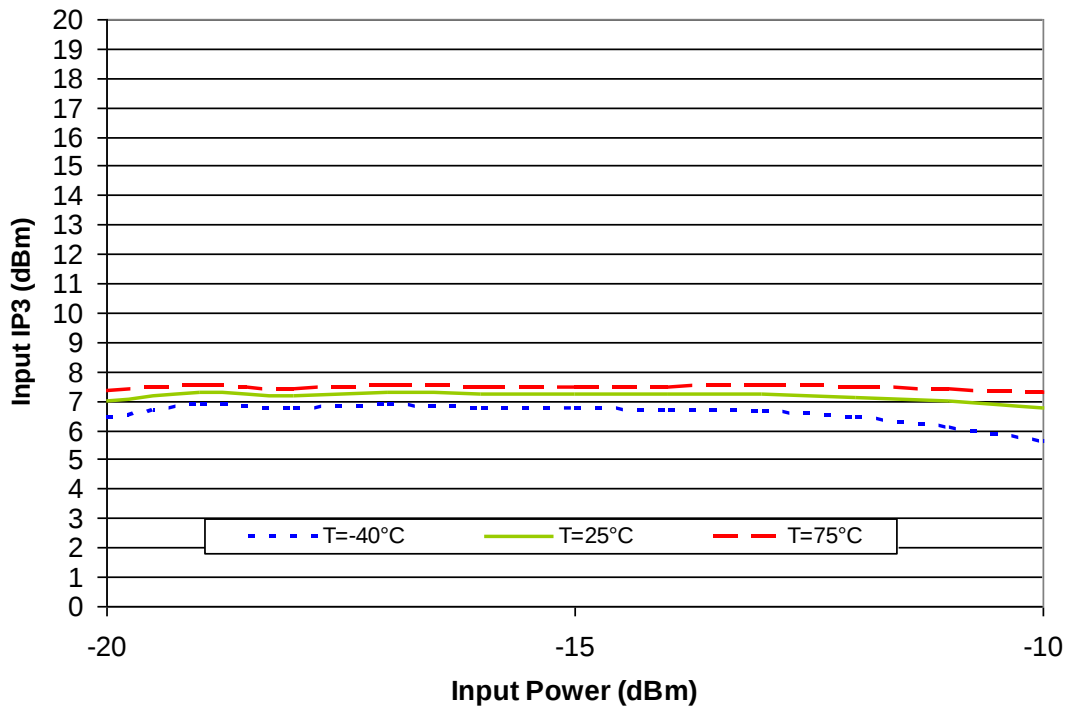


Figure 13: Input IP3 versus Temperature & RF Power (Double Carrier)
 $F_{RF} = 2 \times F_{LO} - F_{IF}$, $F_{RF} = 20.5\text{GHz}$, $F_{IF} = 3.5\text{GHz}$, $GC2 = GC3 = -1.5\text{V}$

The following values are representative of onboard measurements of the Noise Figure where board losses have been deembedded (result given on package access planes).

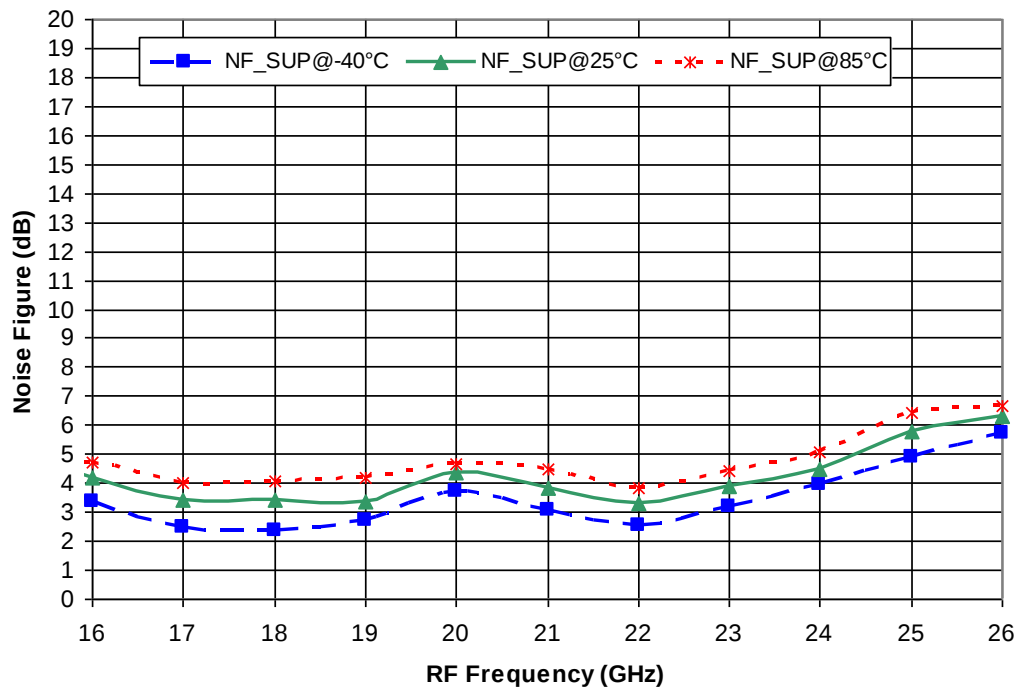


Figure 14: Noise Figure in Supradyn Mode vs Temperature & Frequency
 $F_{RF} = 2 \times F_{LO} + F_{IF}$, $F_{IF} = 2.0\text{GHz}$, $GC2 = GC3 = -1.5\text{V}$

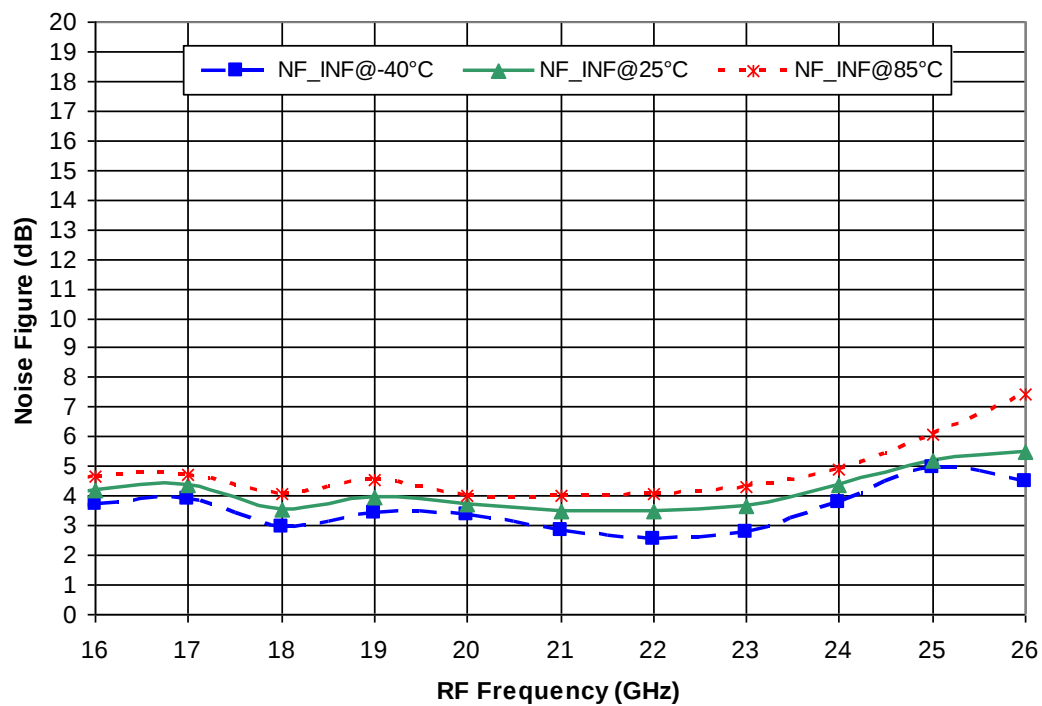
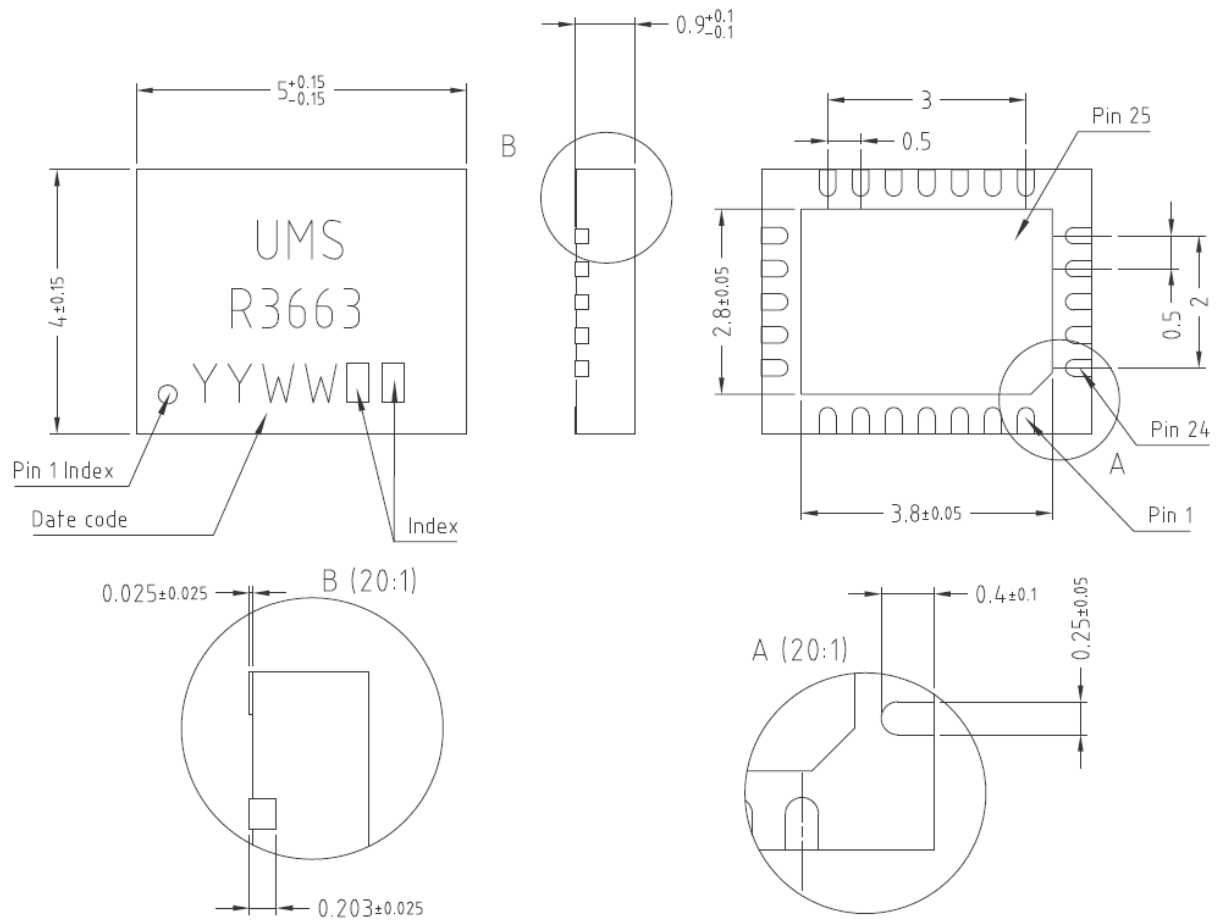


Figure 15: Noise Figure in Infradyne Mode vs Temperature & Frequency
 $F_{RF} = 2 \times F_{LO} - F_{IF}$, $F_{IF} = 2.0\text{GHz}$, $GC2 = GC3 = -1.5\text{V}$

Package outline ⁽¹⁾

Units : mm

From the standard : JEDEC MO-220 [VGHD]

Matt tin, Lead free (Green)

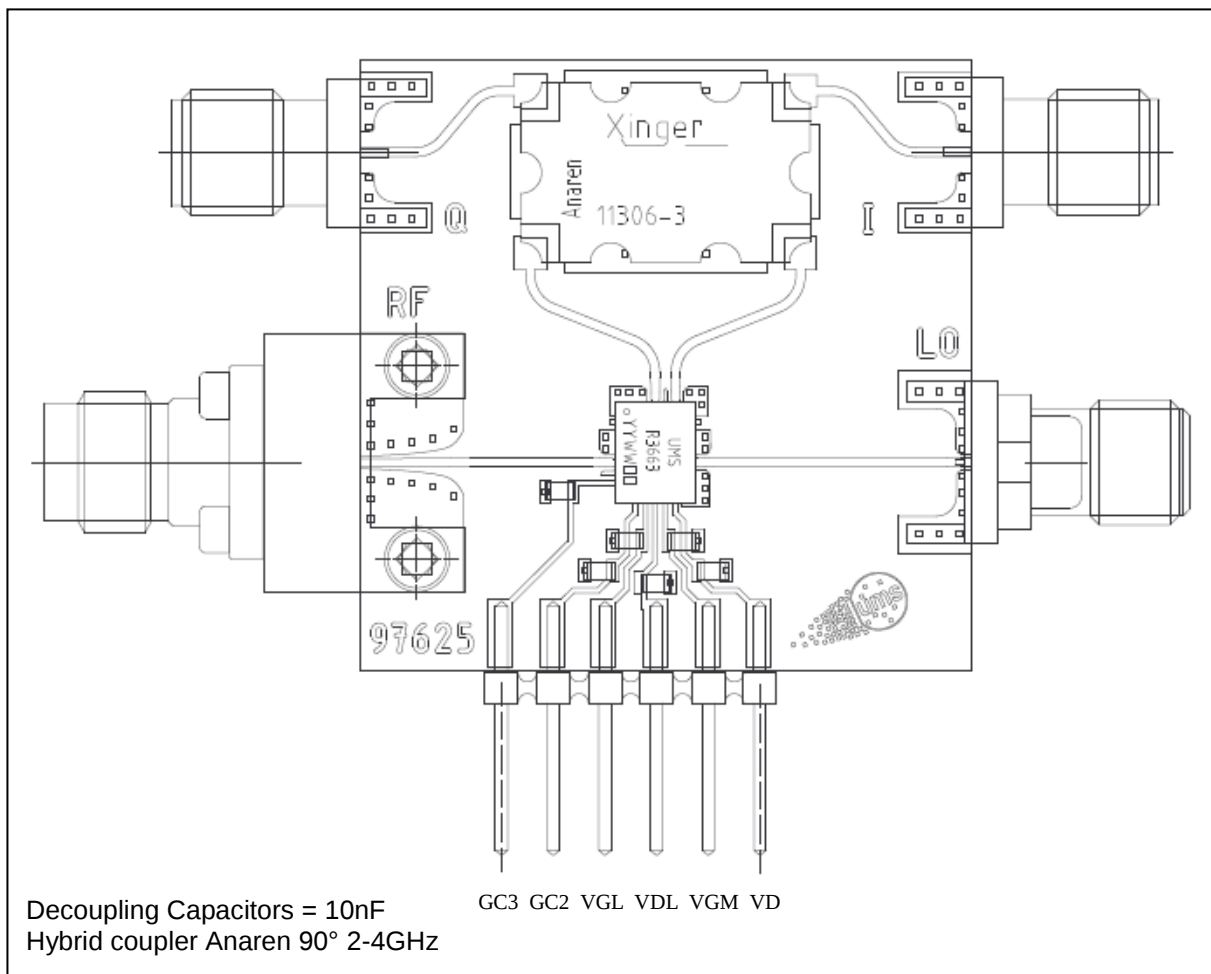
1- Nc	9- VGL	17- Nc	25- GND Exposed pad
2- Nc	10- VDL	18- Nc	
3- Nc	11- VGM	19- Nc	
4- GND ⁽²⁾	12- VD	20- IF_I out	
5- RF in	13- Nc	21- GND ⁽²⁾	
6- GND ⁽²⁾	14- GND ⁽²⁾	22- IF_Q out	
7- GC3	15- LO in	23- Nc	
8- GC2	16- GND ⁽²⁾	24- Nc	

⁽¹⁾The package outline drawing included to this data-sheet is given for indication. Refere to the application note AN0017 available at <https://www.ums-rf.com> for exact package dimensions.

⁽²⁾It is strongly recommended to ground on the PCB board all the pins referenced as GND.

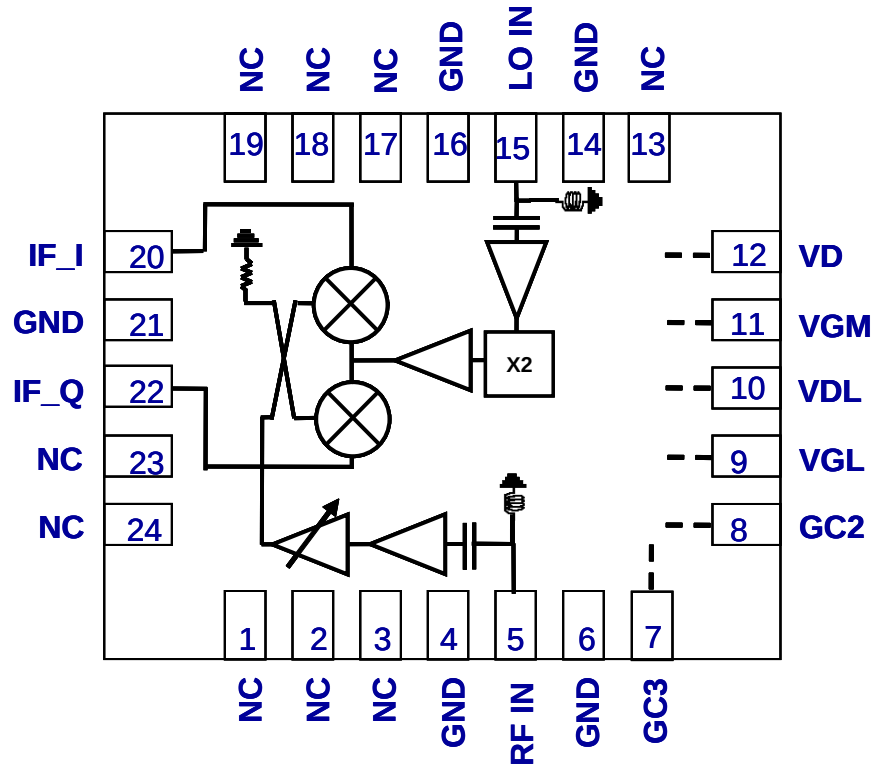
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF $\pm 10\%$ are recommended for all DC accesses.
- (See application note AN0017 for details).



Notes

Due to ESD protection circuits on RF and LO inputs, an external capacitance might be requested to isolate the product from external voltage that could be present on these accesses in the application.



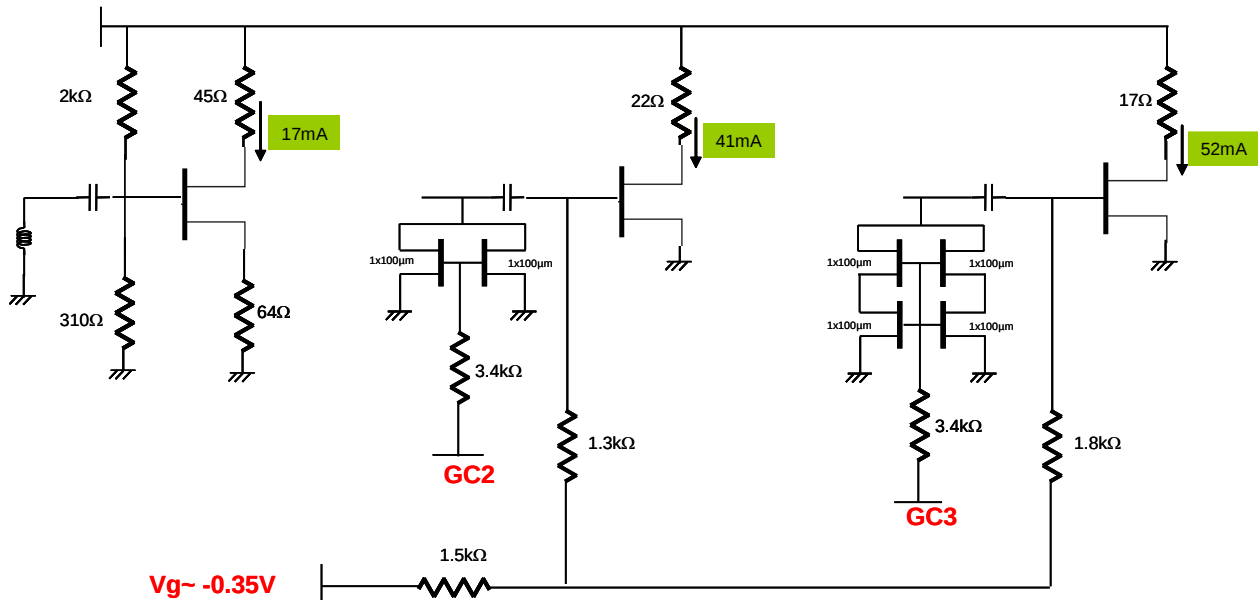
ESD protections are also implemented on gate accesses.

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

DC Schematic

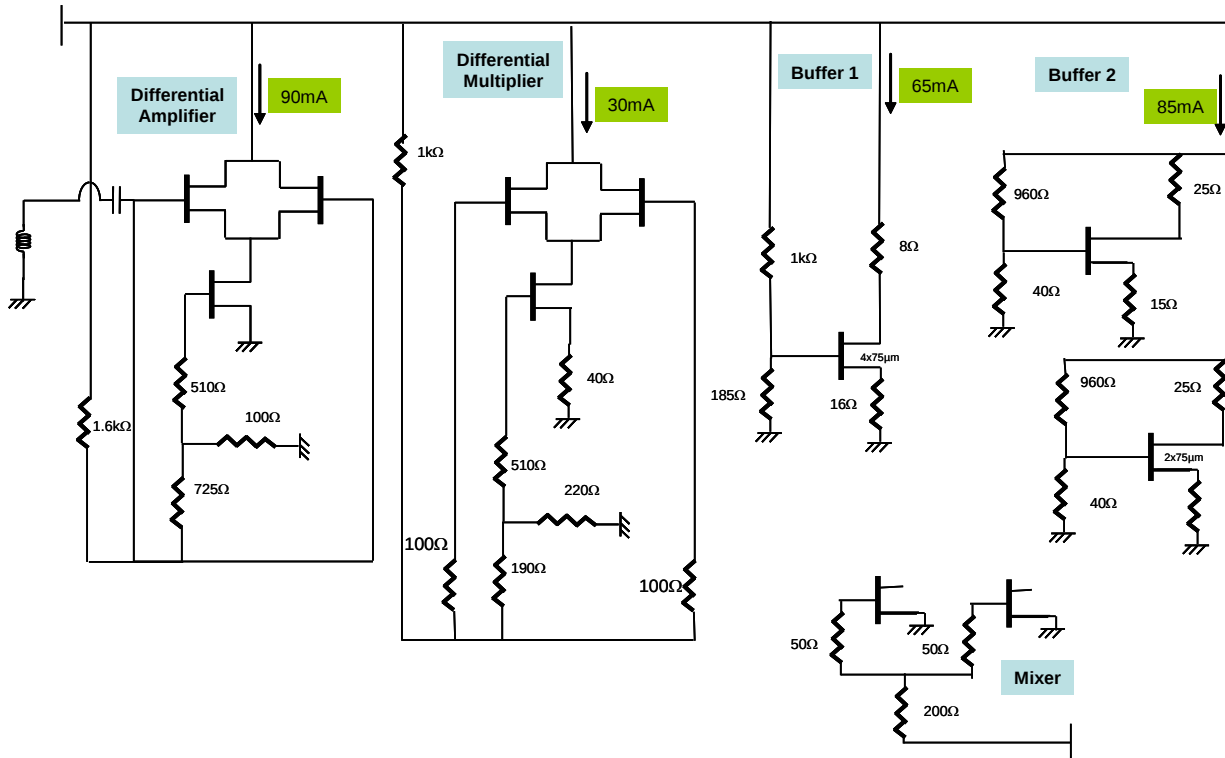
LNA: 4.5V, 110mA

Vd=4.5V, 110mA



LO Buffer: 4.5V, 270mA

Vd= 4.5V, 270mA



Notes:

Recommended package footprint

Refer to the application note AN0017 available at <https://www.ums-rf.com> for package footprint recommendations and exact package dimensions.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at <https://www.ums-rf.com> for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x5 RoHS compliant package: CHR3663-QEG/XY

Stick: XY = 20 Tape & reel: XY = 21

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