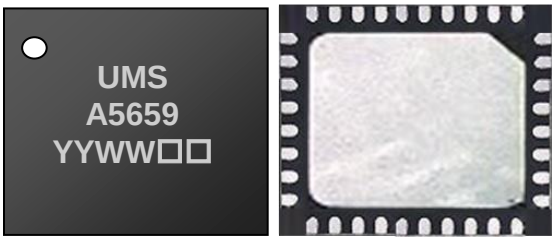
CHA5659-QXG

40-43.5GHz Power Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHA5659-QXG is a four stage monolithic GaAs high power amplifier producing 1 Watt output power. It is highly linear, with possible gain control and integrates a power detector. ESD protections are included.
It is designed for Point To Point Radio or K-band SatCom applications.
The CHA5659-QXG is recommended with the CHA3398-QDG as a driver.
The circuit is manufactured with a pHEMT process, 0.15µm gate length.
It is supplied in RoHS compliant SMD package.

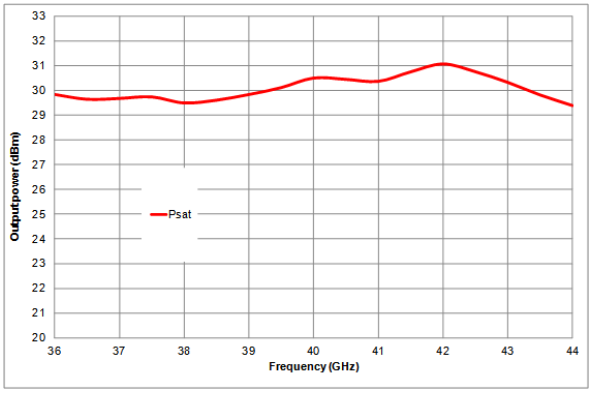


36 leads 6x5mm QFN package

Main Features

- Broadband performances: 40-43.5GHz
- 30dBm saturated power
- 38.5dBm OIP3
- 20dB gain
- DC bias: Vd = 6.0Volt @ Idq = 0.8A
- QFN5x6
- MSL3

Output power vs frequency



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	40.0		43.5	GHz
Gain	Linear Gain		20		dB
Psat	Saturated output power		30		dBm
OIP3	Output IP3		38.5		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +6.0V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	40.0		43.5	GHz
Gain	Small Signal Gain		20		dB
ΔG	Gain variation in temperature		± 0.04		dB/°C
Psat	Saturated Output Power		30		dBm
OIP3	Output IP3		38.5		dBm
PAE	PAE at saturation		15		%
CG	Gain control range		15		dB
Rlin	Input Return Loss		8		dB
Rlout	Output Return Loss		10		dB
Dr	Detection dynamic range(for output power detection up to Psat)		30		dB
Vdetect	Voltage detection V_{REF}- V_{DET} up to Psat		20 to 2000		mV
Vg	DC gate Voltage		-0.65		V
Idq	Total drain current		0.8		A

These values are representative of on-board measurements.
Electrostatic discharge sensitive device observe handling precautions!

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	8	V
Id	Drain bias current	1000	mA
Vg	Gate bias voltage	-2 to 0	V
Pin	Maximum Input Power	+15	dBm
Tj	Maximum Junction temperature (2)	171	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Thermal Resistance channel to ground paddle

Temperature Range

Ta	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
Vd1	7	DC Drain voltage 1st stage	6.0	V
Vd2	6	DC Drain voltage 2nd stage	6.0	V
Vd3	4, 23	DC Drain voltage 3rd stage	6.0	V
Vd4	2, 25	DC Drain voltage 4th stage	6.0	V
Vg1	19	DC Gate voltage 1st stage	-0.65	V
Vg2	21	DC Gate voltage 2nd stage	-0.65	V
Vg3	5, 22	DC Gate voltage 3rd stage	-0.65	V
Vg4	3, 24	DC Gate voltage 4th stage	-0.65	V

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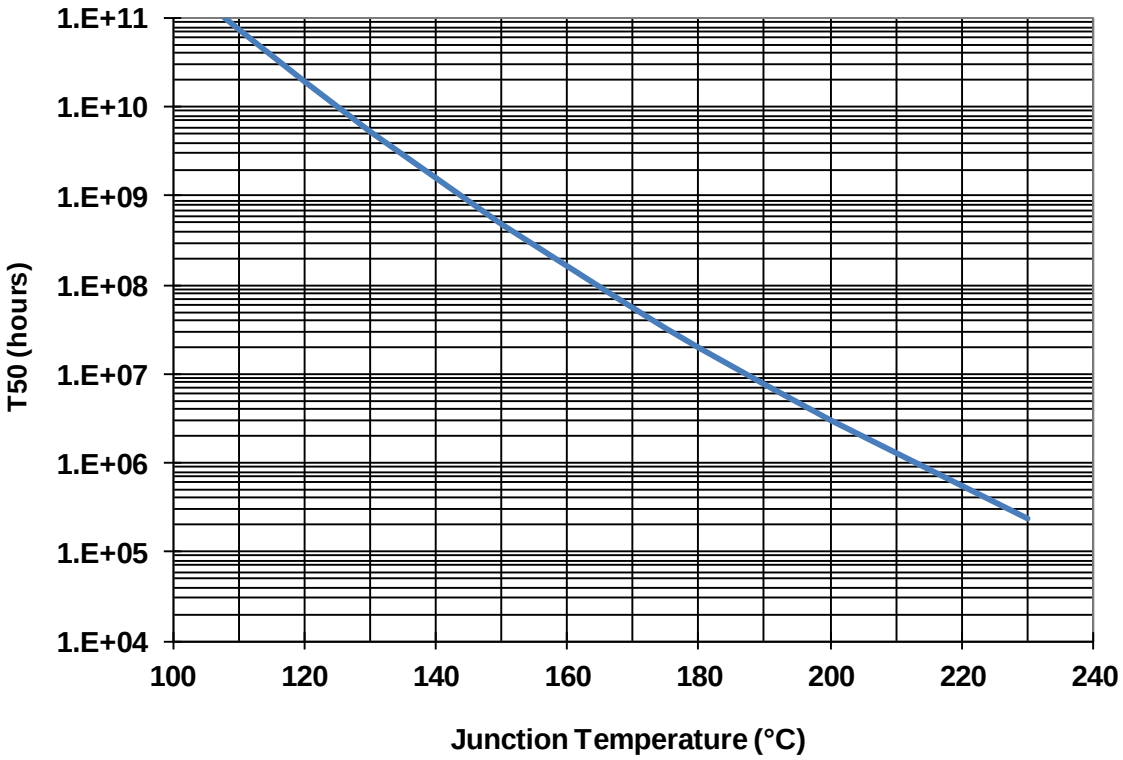
Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	Vd= 6V Idq = 800mA Pdiss= 4.8W	171	17.8	5.3E+07

(1) Assuming 85°C Tcase



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Typical Package Sij parameters

Tamb.= +25°C, Vd = +6.0V, Idq = 800mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S21 (dB)	PhS21 (°)	S12 (dB)	PhS12 (°)	S22 (dB)	PhS22 (°)
5	-0.52	74.54	-67.53	-1.52	-66.88	11.34	-0.33	102.43
6	-0.70	49.57	-64.16	-60.52	-65.02	-17.56	-0.37	85.86
7	-1.03	18.03	-62.40	-146.10	-70.02	-67.49	-0.46	68.64
8	-1.74	-28.09	-48.01	145.09	-77.24	-129.52	-0.60	49.77
9	-2.75	-101.44	-35.46	81.03	-62.86	62.15	-0.82	29.97
10	-2.63	171.22	-26.22	4.83	-62.75	-36.60	-1.26	6.52
11	-1.91	108.89	-17.90	-78.92	-62.71	-138.28	-2.57	-26.75
12	-1.69	67.34	-10.25	-175.87	-53.97	86.92	-9.21	-102.14
13	-1.89	35.65	-7.70	65.79	-51.97	-12.79	-4.85	66.80
14	-2.31	10.88	-9.88	-29.09	-60.03	-54.67	-1.45	11.93
15	-2.59	-10.89	-12.61	-105.14	-78.68	-143.36	-0.84	-19.54
16	-2.69	-31.29	-15.55	-172.76	-64.51	-24.71	-0.67	-44.35
17	-2.68	-51.13	-19.10	134.08	-66.10	150.90	-0.63	-66.35
18	-2.57	-70.36	-21.26	88.39	-54.87	67.67	-0.65	-86.97
19	-2.50	-88.87	-22.77	47.85	-50.71	-3.88	-0.69	-106.37
20	-2.50	-107.28	-23.90	6.03	-55.28	-60.13	-0.70	-125.57
21	-2.42	-125.23	-25.05	-27.64	-51.50	31.84	-0.81	-144.84
22	-2.43	-142.67	-25.75	-63.86	-50.44	2.85	-0.81	-163.70
23	-2.58	-159.63	-27.14	-97.27	-47.40	-19.96	-0.85	176.72
24	-2.53	-177.83	-27.71	-120.16	-43.84	-74.27	-0.98	157.38
25	-2.60	164.64	-28.21	-130.86	-43.17	-81.25	-1.02	137.41
26	-2.81	145.53	-23.97	-132.07	-42.83	-83.24	-1.24	115.95
27	-3.05	125.62	-17.60	-161.53	-43.21	-126.16	-1.43	91.49
28	-3.23	104.16	-11.46	157.21	-42.85	-145.58	-1.84	64.22
29	-3.36	81.73	-5.38	111.75	-44.04	-170.00	-2.58	31.65
30	-3.28	57.64	1.57	57.06	-48.90	-170.91	-3.97	-12.59
31	-3.29	34.13	8.32	-10.10	-46.55	-165.68	-7.09	-75.15
32	-3.41	7.21	13.99	-88.67	-42.25	177.51	-10.56	-169.32
33	-4.07	-18.31	18.40	-171.69	-48.89	172.38	-9.43	111.92
34	-5.33	-48.24	20.92	99.60	-54.68	178.74	-8.88	75.44
35	-8.04	-75.60	21.80	15.26	-47.71	-154.02	-7.61	49.55
36	-14.39	-84.46	22.72	-65.77	-43.83	-170.15	-6.98	28.93
37	-14.30	-53.69	22.78	-146.65	-39.52	-174.93	-5.79	6.59
38	-15.07	-72.87	22.43	134.96	-38.54	158.26	-5.97	-19.48
39	-19.08	-85.29	22.09	58.12	-39.62	135.69	-7.86	-42.64
40	-20.44	-178.75	21.76	-19.97	-37.14	144.47	-11.06	-63.27
41	-13.55	87.64	20.56	-98.81	-34.53	127.15	-21.82	-64.28
42	-9.79	26.41	20.13	-169.60	-32.42	117.13	-13.81	4.03
43	-7.06	-28.15	22.02	114.81	-28.47	97.79	-8.21	-41.42
44	-3.66	-174.16	25.54	-12.67	-23.21	37.94	-2.72	165.93
45	-3.60	69.27	15.59	-140.93	-27.82	-7.55	-2.16	40.20

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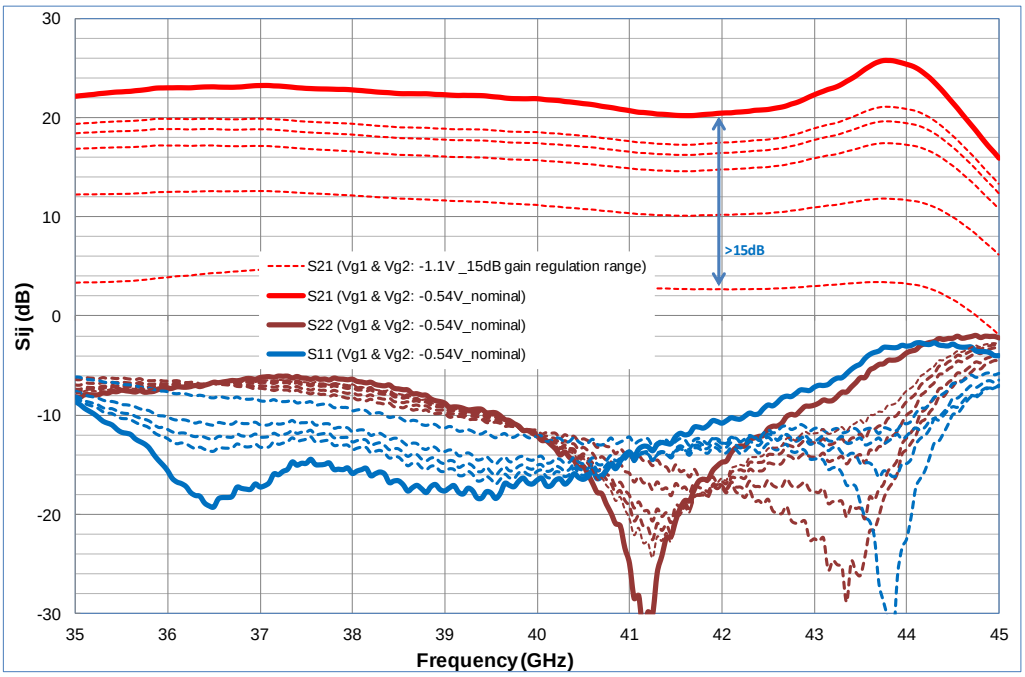
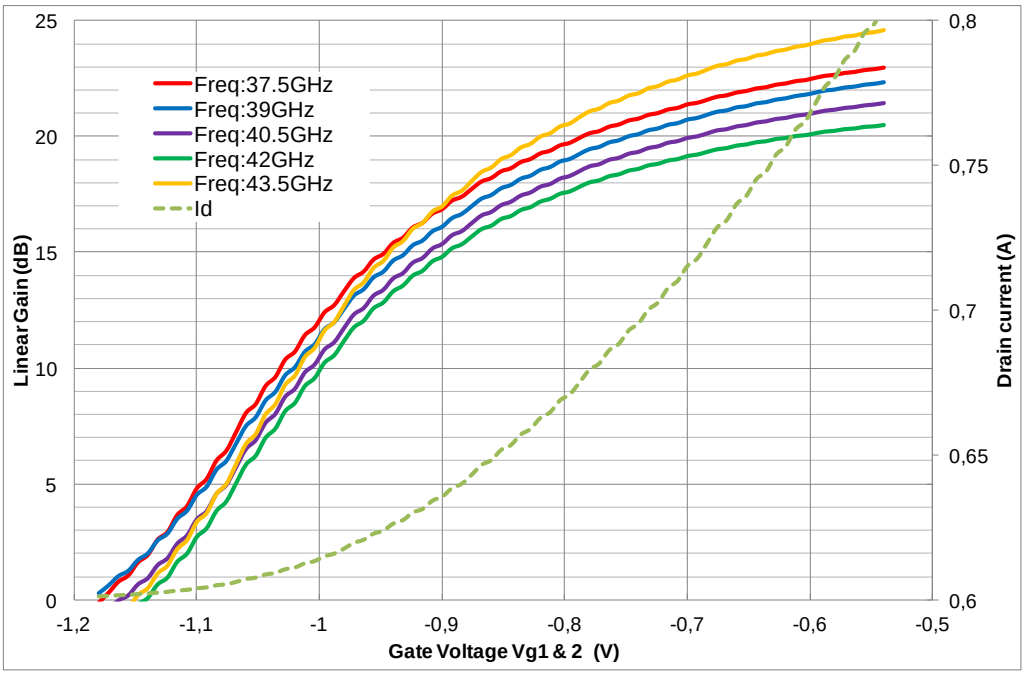
Typical Board Measurements on a probe compatible Board

Tamb.= +25°C, Vd = +6.0V, Idq = 800mA
Measurement in the plan of the QFN, using the proposed land pattern & board, as defined in paragraph “Evaluation mother board”

Gain & Return Loss versus Frequency & Gate Voltage (Vg1 & 2)



Gain control & current versus Gate Voltage (Vg1 & 2)



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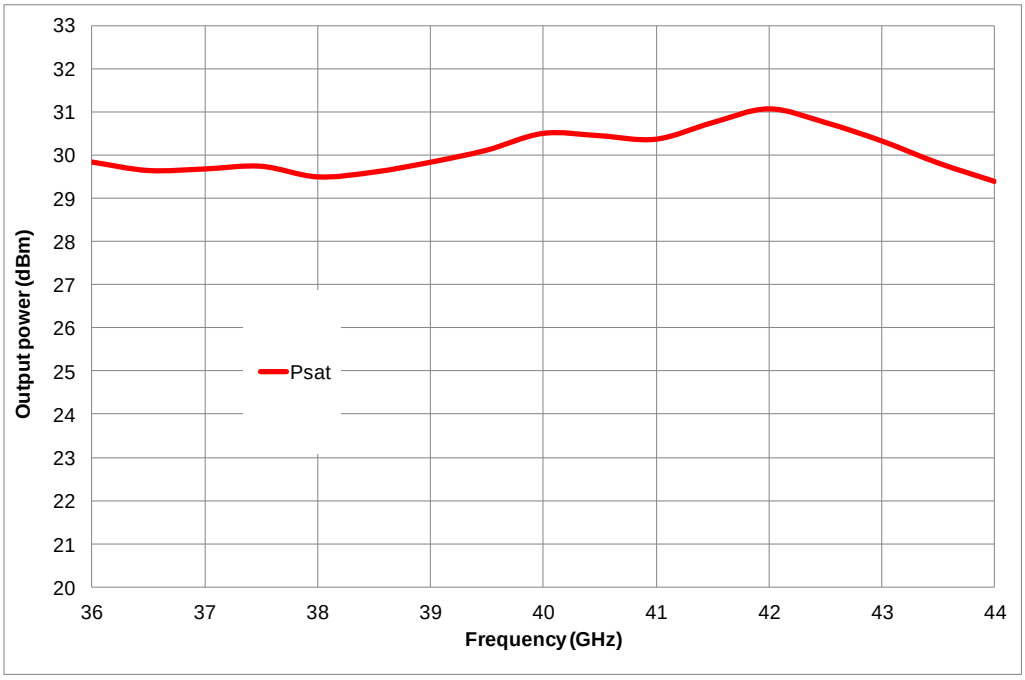
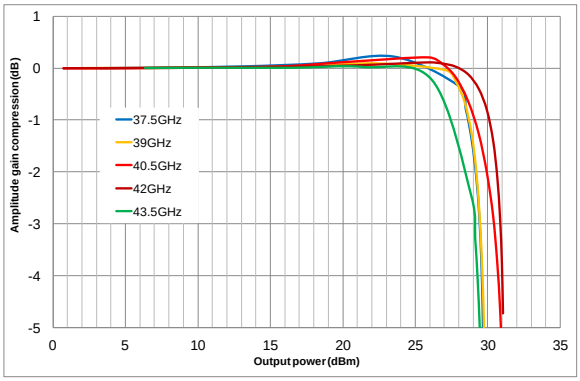
Typical Measurements on a probe compatible Board

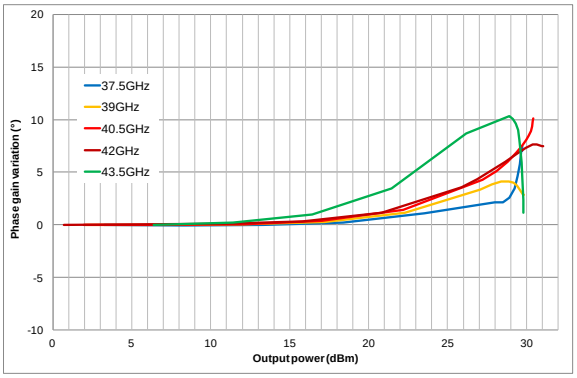
Tamb.= +25°C, Vd = +6.0V, Idq = 800mA

Output Power versus Frequency

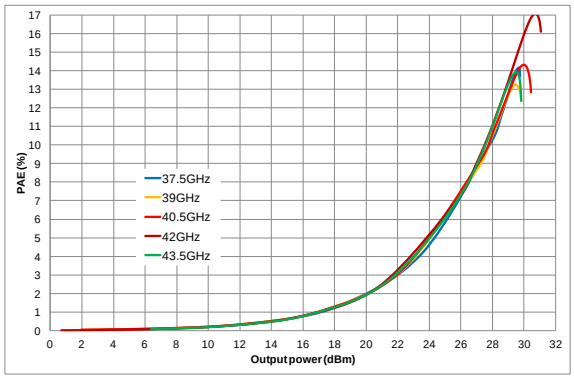


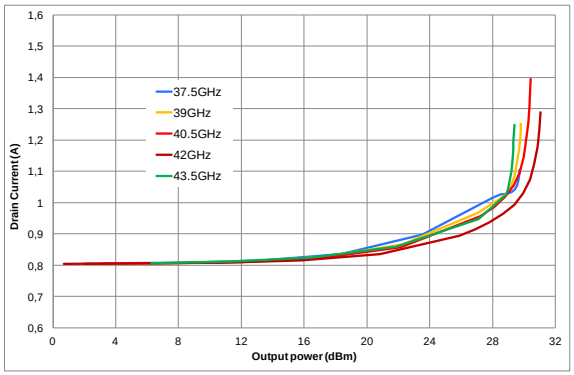
Amplitude & Phase variation versus Output Power





PAE & Drain Current versus Output Power





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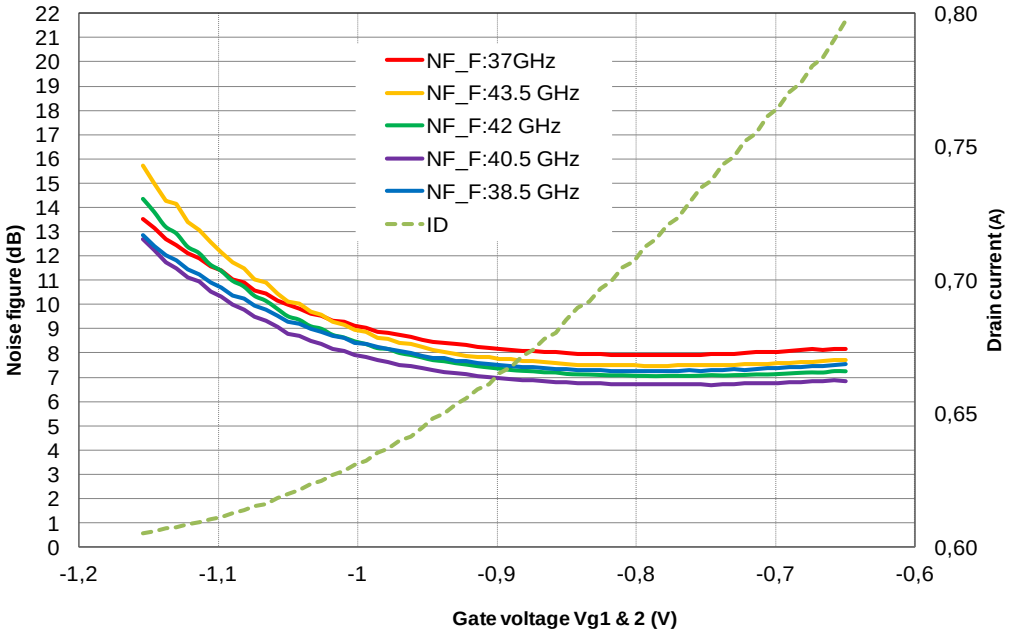
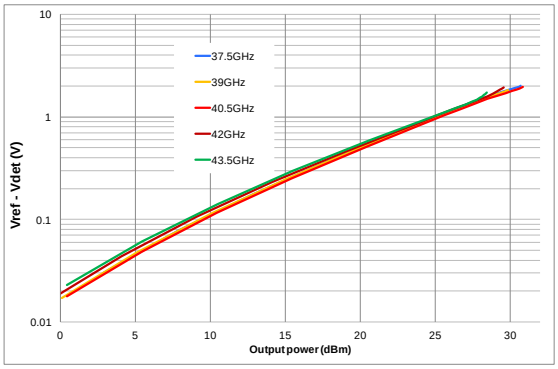
Typical Board Measurements

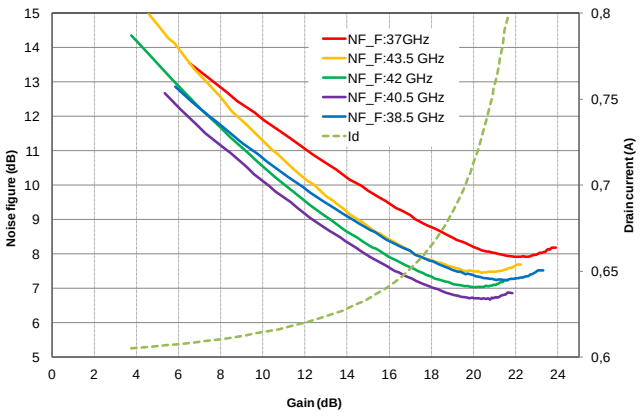
Tamb.= +25°C, Vd = +6.0V, Idq = 800mA

Noise Figure variation versus Gate Voltage

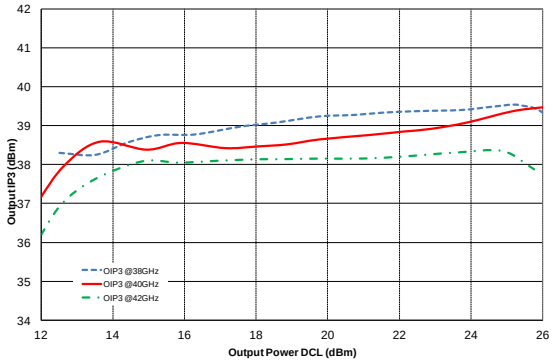


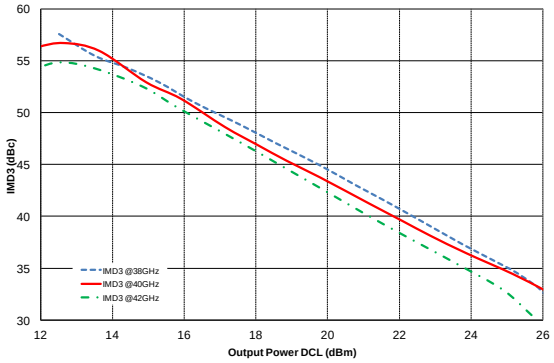
Power Detector versus Output power & Noise Figure versus Gain Control





Output IP3 & IMD3 versus Output Power





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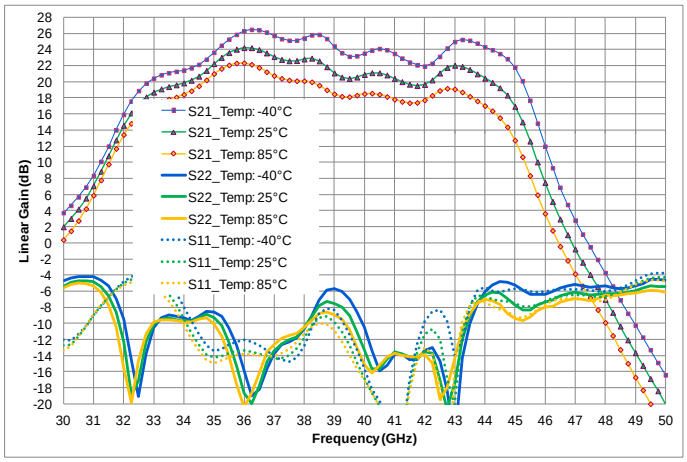
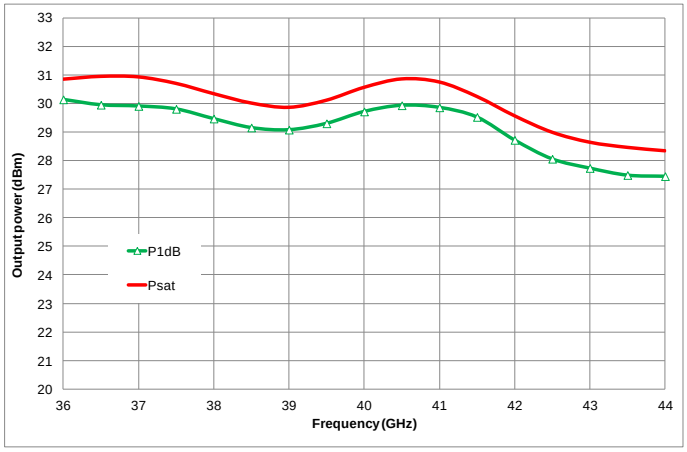
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Idq = 800mA

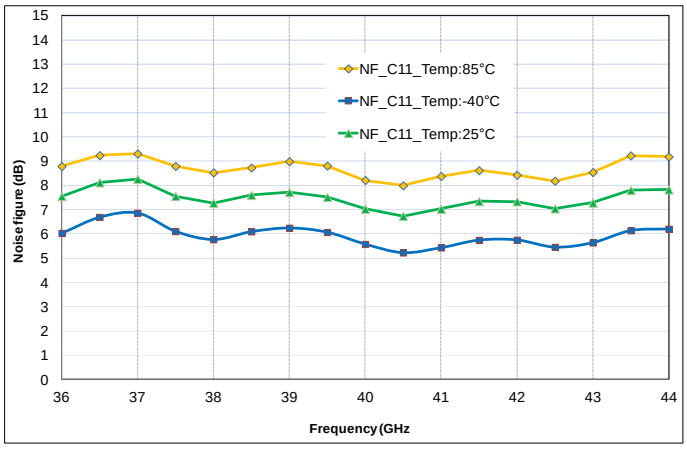
Gain variation versus Temperature



Output Power versus Frequency



Noise Figure versus Temperature



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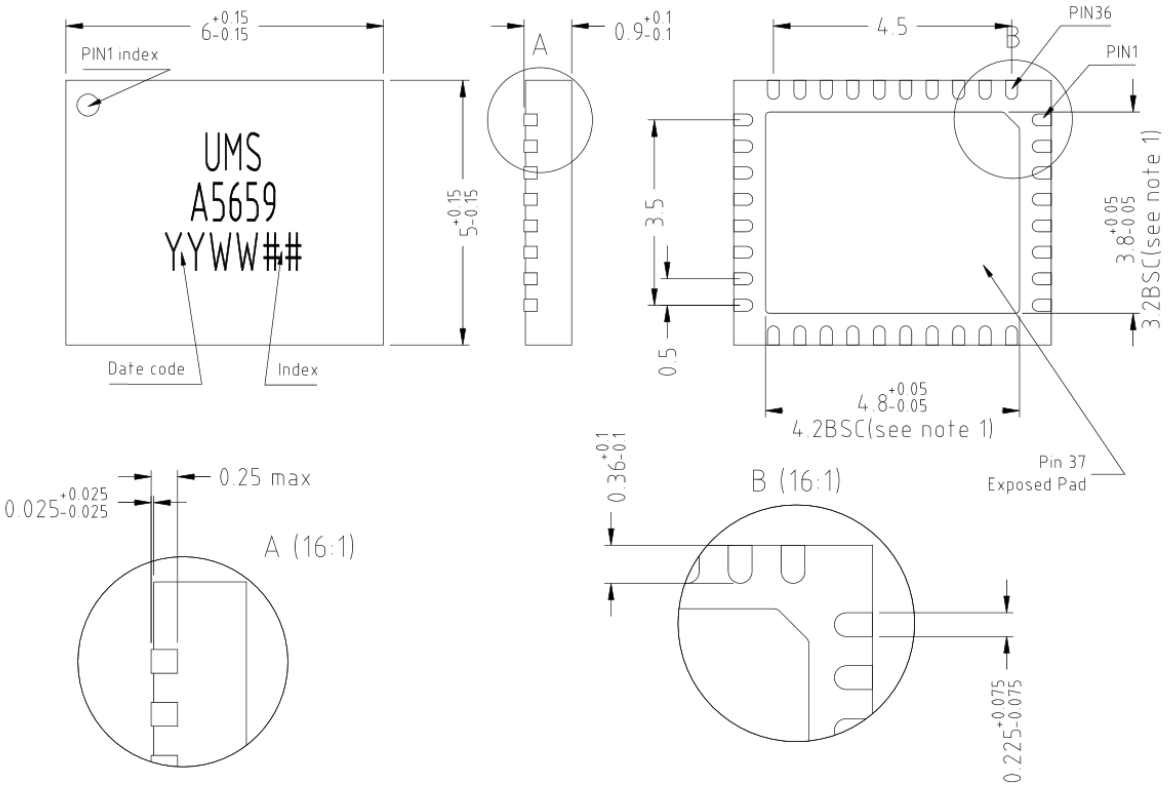
Package outline (1)



Matte tin, Lead Free (Green)	1- DET	13- Gnd(2)	25- Vd4
Units : mm	2- Vd4	14- RF in	26- NC
From the standard : JEDEC MO-220	3- Vg4	15- Gnd(2)	27- Gnd(2)
(VGGD)	4- Vd3	16- NC	28- NC
37- GND	5- Vg3	17- NC	29- NC
	6- Vd2	18- NC	30- Gnd(2)
	7- Vd1	19- Vg1	31- RF out
	8- NC	20- NC	32- Gnd(2)
	9- NC	21- Vg2	33- NC
	10- NC	22- Vg3	34- NC
	11- NC	23- Vd3	35- NC
	12- NC	24- Vg4	36- REF

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (https://www.ums-rf.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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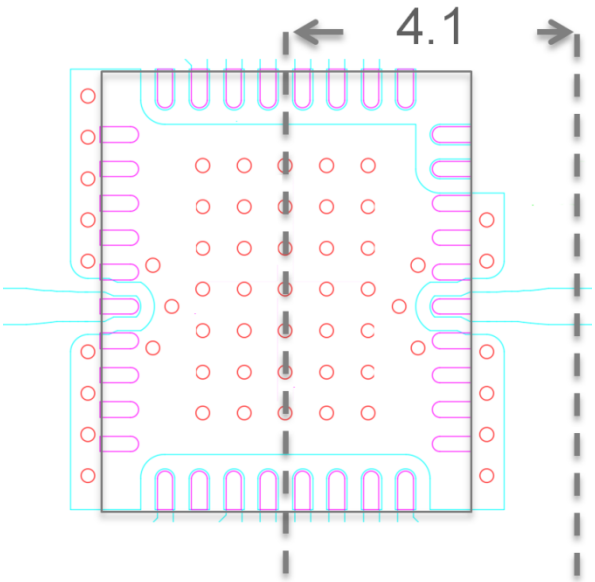
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 4.1mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



ESD sensitivity

Standard	Value
MIL-STD-1686C	HBM Class 1 (<2000V)

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL3

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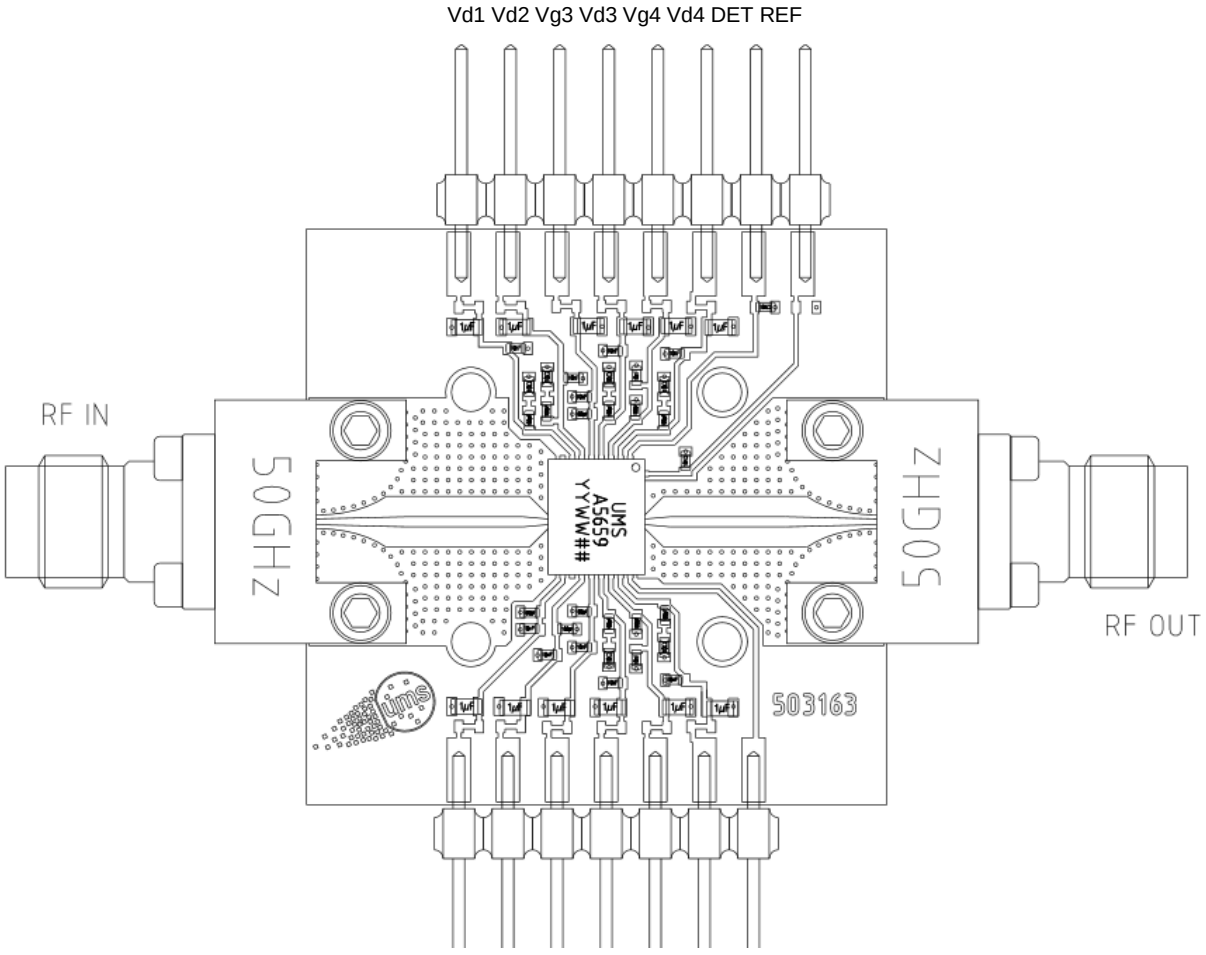
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4350B / 10mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF ±5%, 10nF ±10% and 1µF ±10% are recommended for the gate accesses.
- Decoupling capacitors of 100pF ±5% in series with 10ohms ±1%, 10nF ±10% and 1µF ±10% are recommended for the drain accesses.
- A 10KΩ resistor is recommended on VREF & VDET accesses for the detector
- See application note AN0017 for details.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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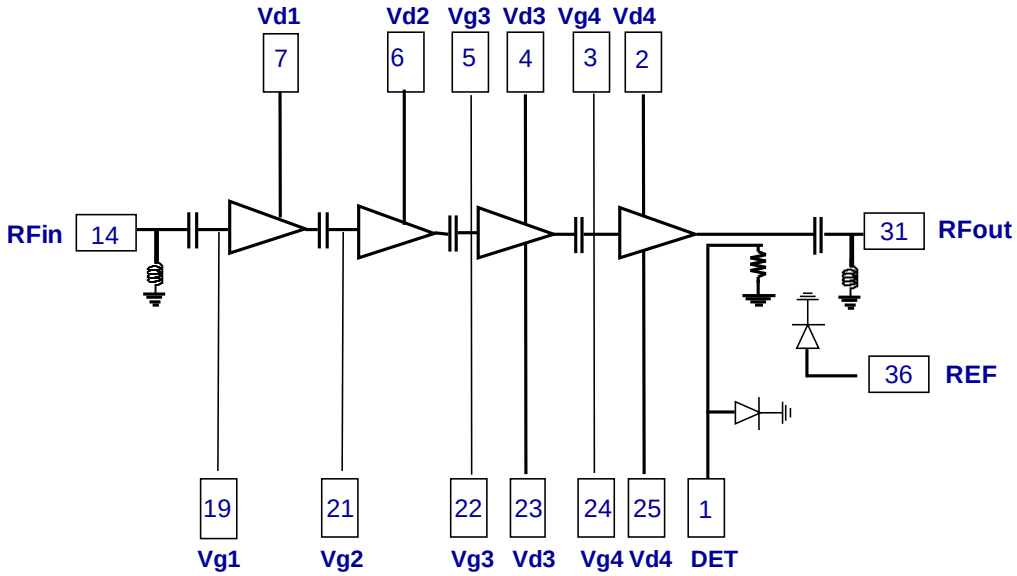
Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF, 10nF, 1µF) on the PC board, as close as possible to the package.

A 10KΩ resistor is recommended in parallel to VDET, and VREF accesses.

The circuit includes ESD protections on all RF and DC leads

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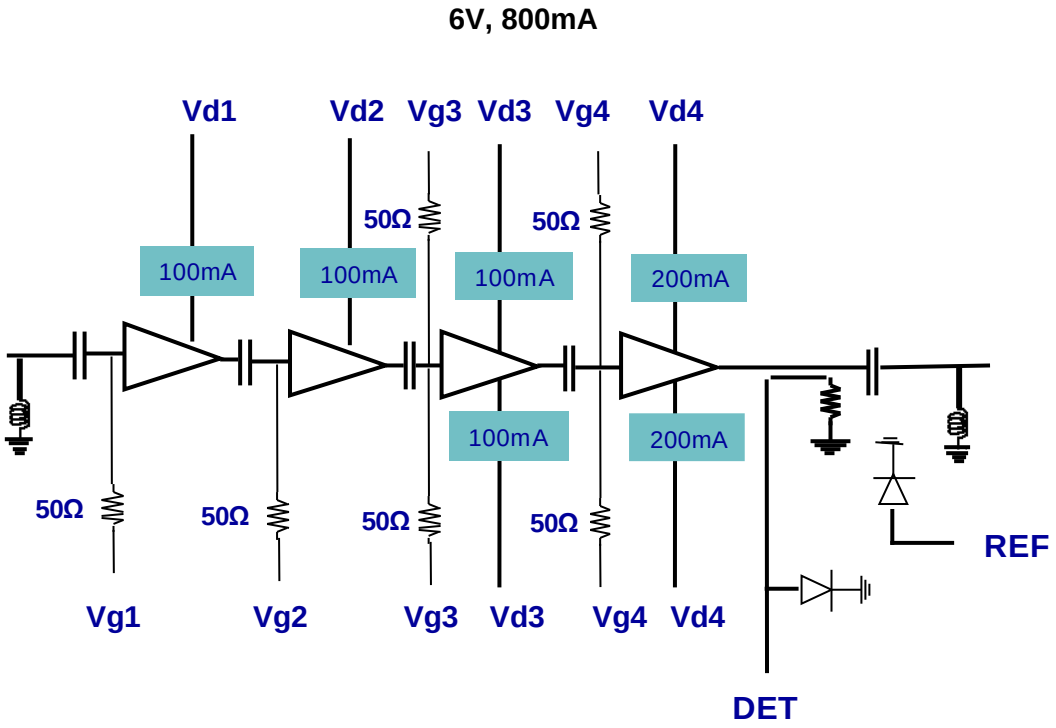
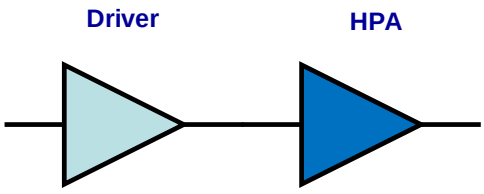
DC Schematic



Recommended UMS Power chain

The CHA5659-QXG is recommended with the CHA3398-QDG as driver.
Total Gain: 42dB
Gain control: 30dB with the both amplifiers.
For more information about CHA3398-QDG, see our web site.



CHA3398-QDG
36- 43.5GHz
4V
200mA

CHA5659-QXG
40- 43.5GHz
6V
800mA

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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 6x5 package:	CHA5659-QXG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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