CHR2295-99F

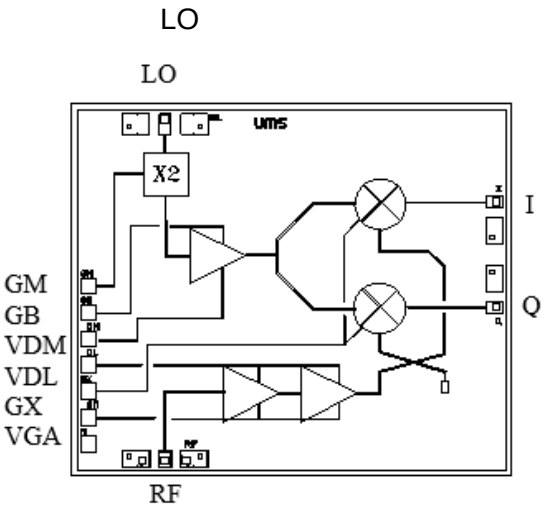
24-30GHz Integrated Down Converter

GaAs Monolithic Microwave IC

Description

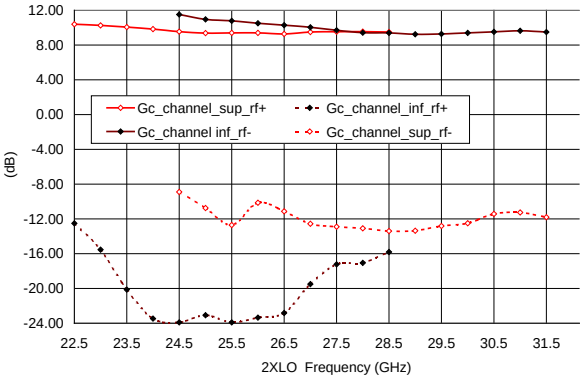
The CHR2295-99F is a multifunction chip which integrates a LO time two multiplier, a balanced cold FET mixer, and a RF LNA. It is designed for a wide range of applications, typically commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Main Features

- Broadband performances: 24-30GHz
- 11dB conversion gain
- 3.5dB noise figure, for IF>0.1GHz
- 10dBm LO input power
- -10dBm RF IP@1dB gain comp.
- Low DC power: 120mA@3.5V
- Chip size: 2.49x1.97x0.10mm



Conversion Gain & Image suppression
@IF=1.5GHz (test board losses included)

Main Electrical Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	24		30	GHz
F_{LO}	LO frequency range	12		15	GHz
F_{IF}	IF frequency range	DC		1.5	GHz
G_c	Conversion gain	8.5	11		dB

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Electrical Characteristics for Broadband Operation

Tamb = +25°C, Vd = 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	24		30	GHz
F_{LO}	LO frequency range	12		15	GHz
F_{IF}	IF frequency range	DC		1.5	GHz
G_c	Conversion gain (1)	8.5	11		dB
NF	Noise Figure, for IF>0.1GHz		3.5		dB
P_{LO}	LO Input power		10		dBm
Img Sup	Image Suppression	15	17		dBc
P1dB	Input power at 1dB gain compression		-10		dBm
LO VSWR	Input LO VSWR (1)		2.0:1		
RF VSWR	Input RF VSWR (1)		3.0:1		
Id	Bias current (2)		120		mA

(1) On Wafer measurements
(2) Current source biasing network is recommended. Optimum performances will be achieved for Idm=50mA and Idl=70mA

Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.0	V
Id	Drain bias current	200	mA
Vg	Gate bias voltage	-2.0 to +0.4	V
Pin	Maximum peak input power overdrive (2)	+15	dBm
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

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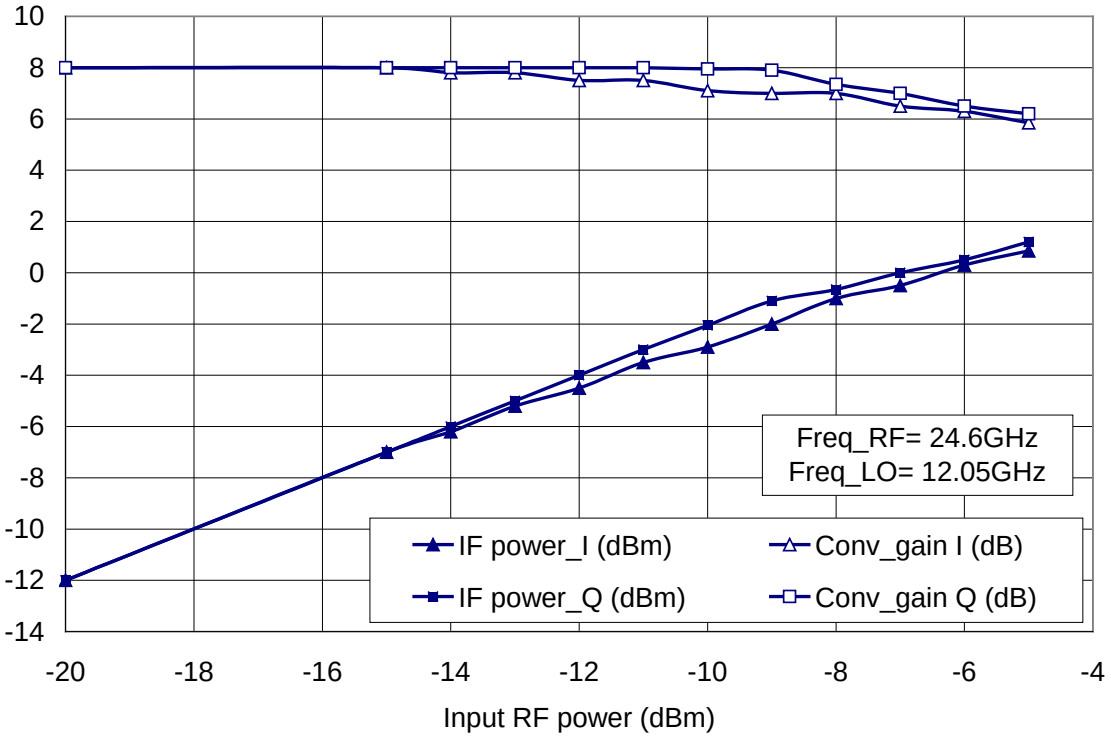
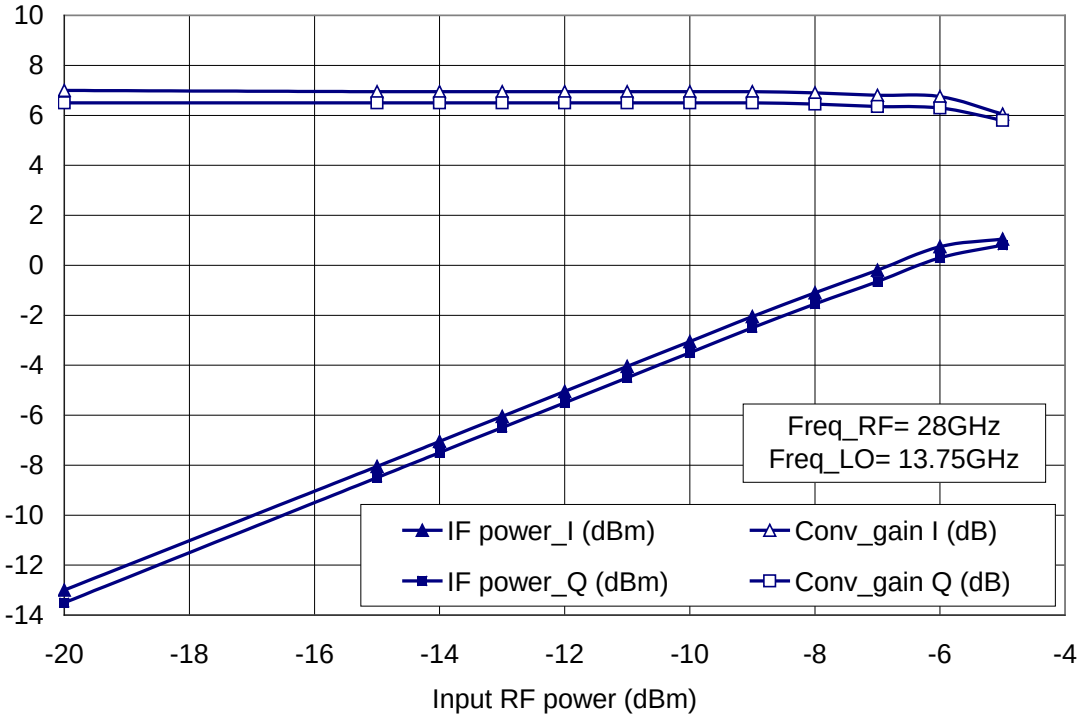
Typical On-wafer Measurements

Bias Conditions : Vdm= Vdl= 3.5V, Vgm= -0.9V, Vgb= -0.3V, Vgx= -0.7V, Vga= -0.2V





Input RF compression by channel

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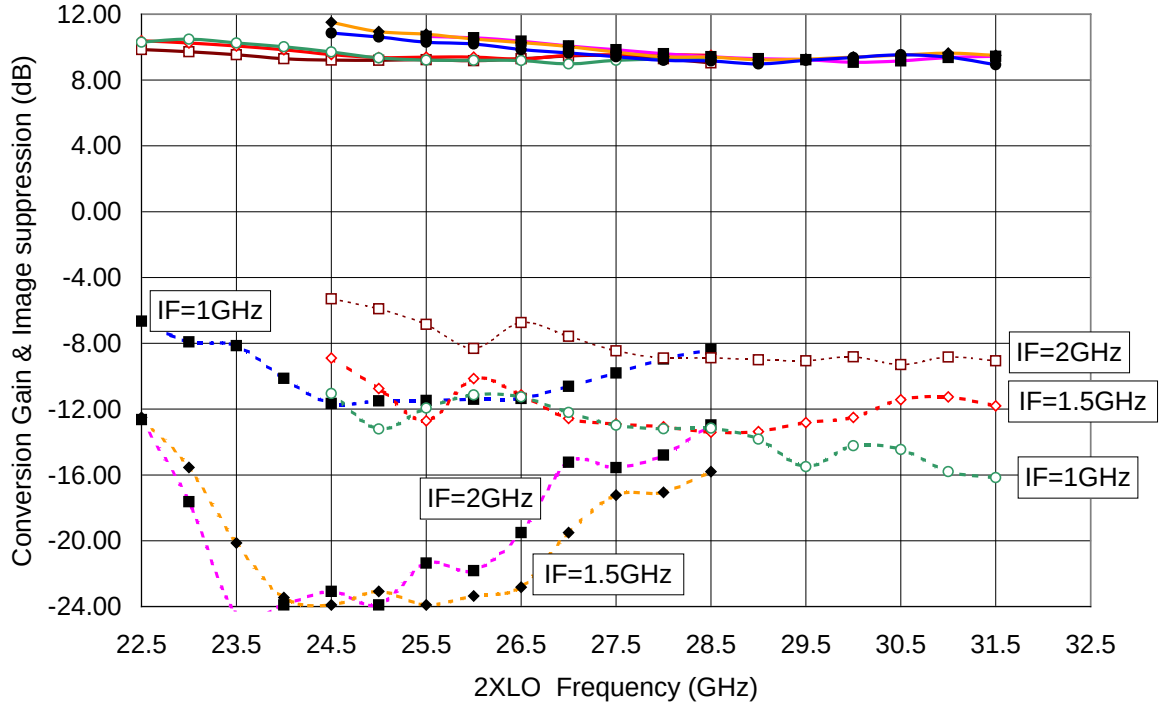
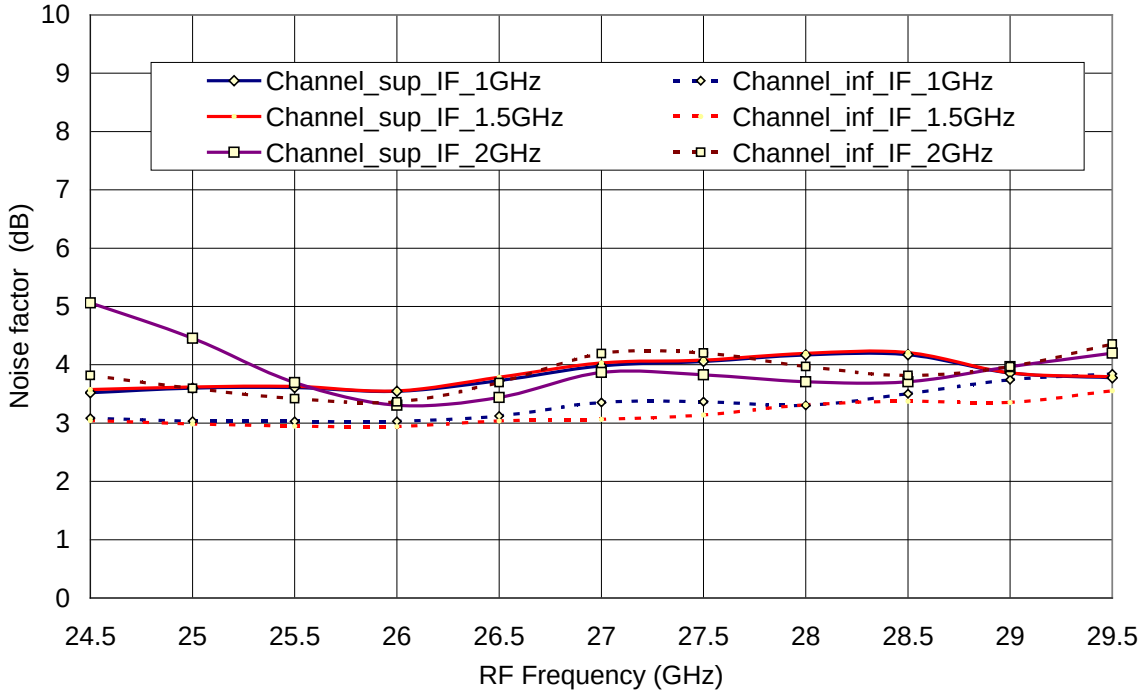
Typical On-board Measurements

Bias Conditions : Vdm= Vdl= 3.5V, Vgm= Vgx= -0.9V, Vgb= Vga= -0.3V

All these measurements include the losses from the test board (typically 1dB for the conversion gain and 0.5dB for the Noise Figure).



Conversion gain & Image suppression versus IF frequency



Noise figure supradyne & infradyne versus IF frequency

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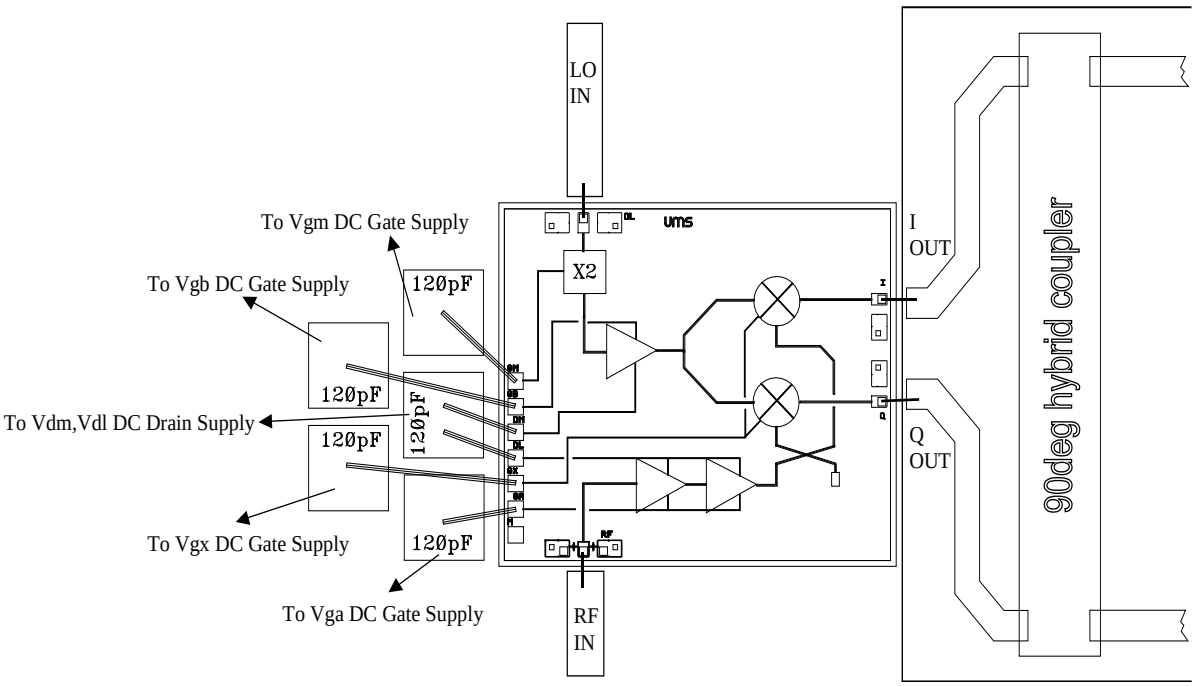
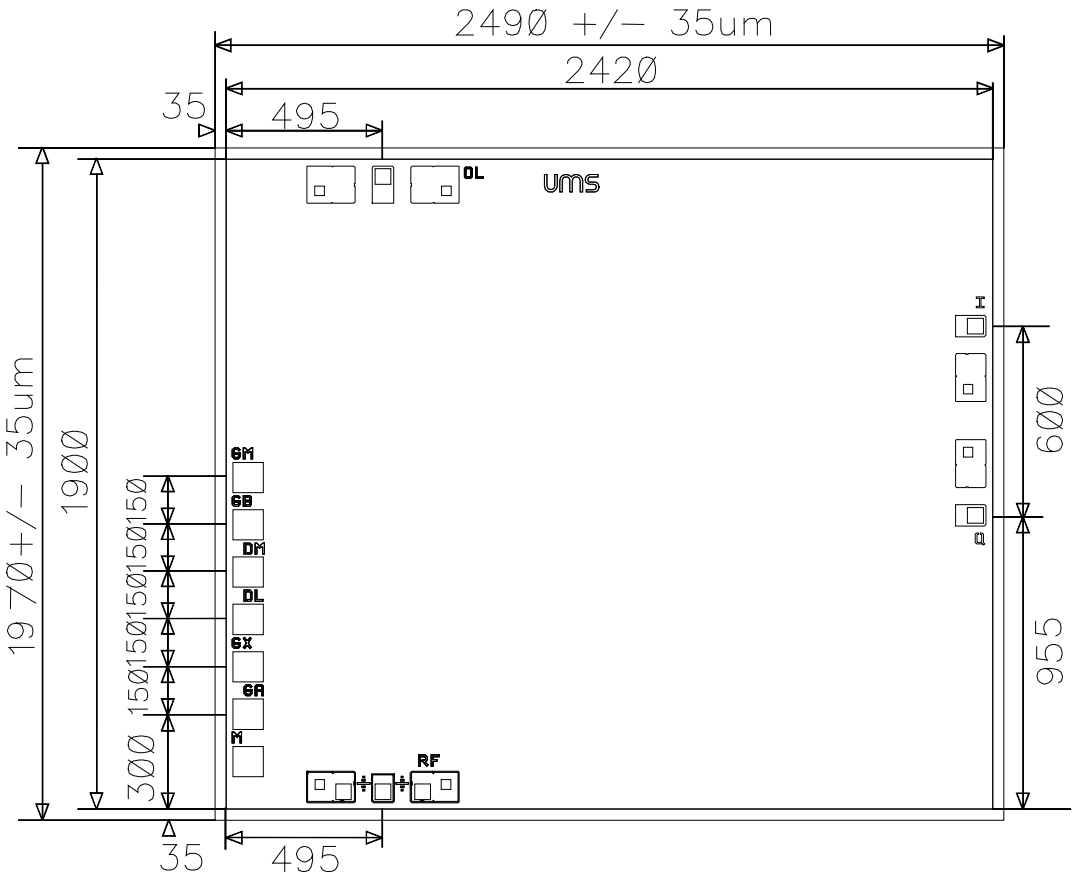
Chip Assembly and Mechanical Data



Note: Supply feed should be bypassed. 25µm diameter gold wire is recommended



Bonding pad positions
(Chip thickness: 100µm. All dimensions are in micrometers)

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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

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