United Monolithic Semiconductors

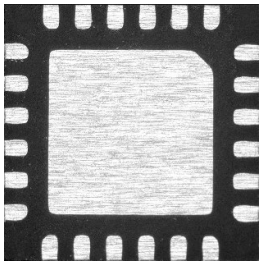
CHA6251-QKB

17 – 21.5GHz 5W Power Amplifier

GaN Monolithic Microwave IC in SMD leadless package

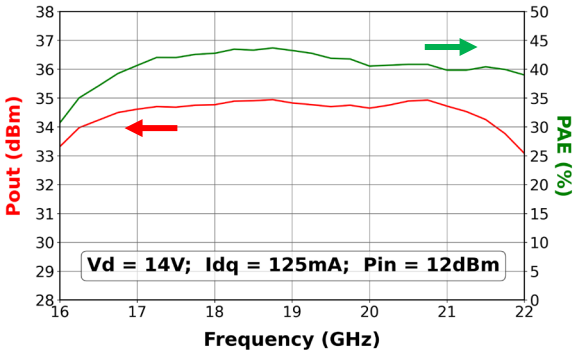
Description

The CHA6251-QKB is a three-stage power amplifier operating in the 17 – 21.5GHz frequency range.
Depending on the biasing point, it can provide between 33dBm and 37dBm of output power associated with 42% Power Added Efficiency on average across the frequency band.
This power amplifier operates on a 12 – 20V supply with a drain current of 60 – 250mA.
Designed for space applications, it is also ideal for a wide range of microwave systems.
The product is developed on a robust GaN on SiC HEMT process and is provided on low cost SMD RoHS compliant QFN plastic package.



Main Features

- 17 – 21.5 GHz frequency range
- Linear Gain is more than 30dB
- 34.5dBm Pout @Vd = 14V @Max_PAE
- Associated PAE = 42%
- DC bias: Vd = 14V @Idq = 125mA
- 24 Leads – QFN 4x4mm^2
- MSL3



Main Electrical Characteristics

Test conditions : T_{case} = 25°C, Vd = 14V, Idq = 125mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17		21.5	GHz
Gain	Linear Gain		33		dB
Pout	Saturated output Power (Pin = 12dBm)		34.5		dBm
PAE	Power Added Efficiency (Pin = 12dBm)		42		%

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Specifications

Test conditions : T_{case} = 25°C, Vd = 14V, Idq = 125mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17		21.5	GHz
Gain	Linear Gain		33		dB
Pout	Saturated output Power (Pin = 12dBm)		34.5		dBm
PAE	Power Added Efficiency (Pin = 12dBm)		42		%
Id	Drain current at saturation (Pin = 12dBm)		500		mA
S11	Input Return Loss		12		dB
S22	Output Return Loss		10		dB

Test conditions : T_{case} = 25°C, Vd = 20V, Idq = 125mA

Symbol	Parameter	Min	Typ	Max	Unit
Gain	Linear Gain		36		dB
Pout	Saturated output Power (Pin = 12dBm)		37		dBm
PAE	Power Added Efficiency (Pin = 12dBm)		37		%
Id	Drain current at saturation (Pin = 12dBm)		650		mA

These values are representative of on board measurements as defined on the drawing in paragraph "Evaluation mother board".

Recommended Operating Range (1), (2)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage range	12 – 20	V
Idq	Drain quiescent current	60 – 250	mA
$T_{junction}$	Maximum junction temperature	200	°C
Pin	Maximum peak input power overdrive @60mA	16	dBm
Pin	Maximum peak input power overdrive @125mA	14	dBm
Pin	Maximum peak input power overdrive @250mA	12	dBm

(1) Electrical performances are defined for specified test conditions

(2) Electrical performances are not guaranteed over all recommended operating conditions

Recommended Operating Range for Space Application (1), (2)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage range	12 – 16	V
Idq	Drain quiescent current	60 – 125	mA
$T_{junction}$	Maximum junction temperature	160	°C
Pin	Maximum peak input power overdrive @60mA	16	dBm
Pin	Maximum peak input power overdrive @125mA	14	dBm

(1) Electrical performances are defined for specified test conditions

(2) Electrical performances are not guaranteed over all recommended operating conditions

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Absolute Maximum Ratings (3)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Vg	Gate bias voltage	-7 to -1.5	V
Idq	Drain quiescent current	1300	mA
Pin	Maximum peak input power overdrive @60mA	17	dBm
Pin	Maximum peak input power overdrive @125mA	15	dBm
Pin	Maximum peak input power overdrive @250mA	13	dBm
T_{case}	Operating temperature range	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

(3) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Symbol	Pad N°	Parameter	Values	Unit
Vd	19; 20; 22	Drain bias voltage	12 – 20	V
Vg	8; 10; 11	Gate bias voltage	Set Vg for recommended Idq	V

"Power ON" sequence

1. Bias PA gate voltage at Vg close to $V_{pinch-off}$ (Typically: Vg ≈ -5V)
2. Apply Vds bias voltage (Typically: Vd = 14V)
3. Increase Vgs up to quiescent bias drain current Idq (pulsed applied on the gate)
4. Apply RF signal

"Power OFF" sequence

1. Turn off RF signal
2. Bias PA gate voltage at Vg close to $V_{pinch-off}$ (Typically: Vg ≈ -5V)
3. Turn Vds bias voltage to 0V
4. Turn Vgs bias voltage to 0V

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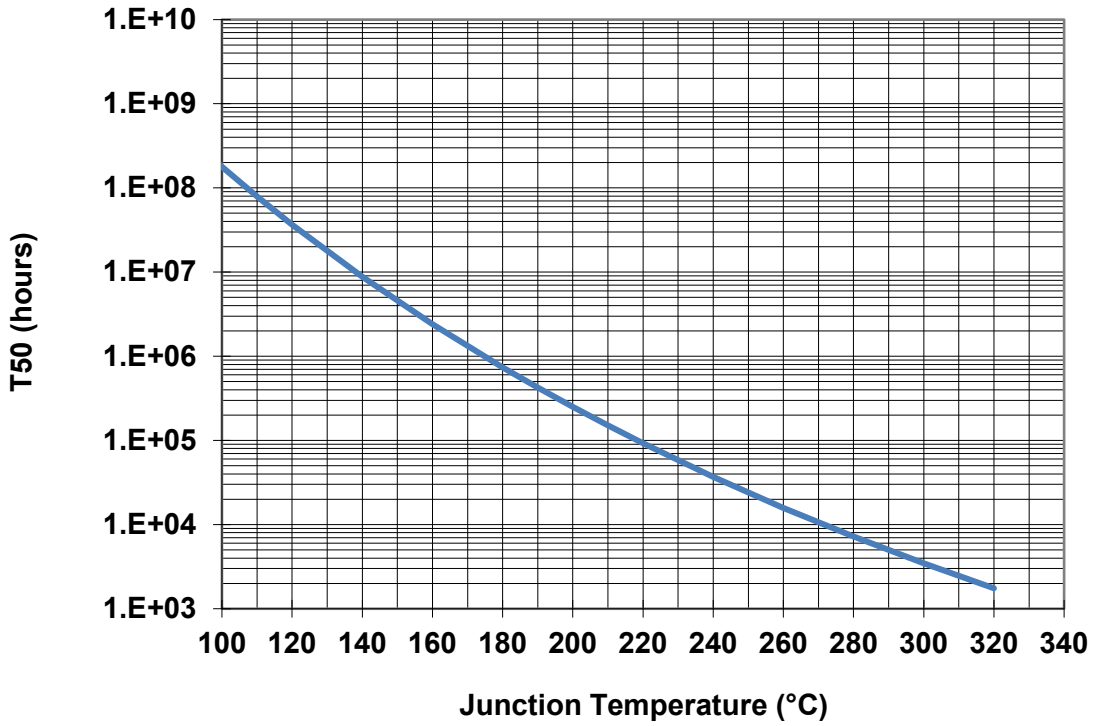
Device Thermal Performances

All the figures given in this section are obtained assuming that the die is only cooled down by conduction through the package case.
The temperature is monitored at the QFN backside interface (T_{case}).
For nominal operation, the system's maximum temperature must be adjusted to ensure that the junction temperature ($T_{junction}$) remains below the maximum value specified in the Recommended Operating Ratings table.
The system PCB must be designed to comply with this requirement.

Parameter	Conditions	$T_{junction}$ (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	Vd = 12V Pout = 32.5dBm Pdiss = 3.9W	126	10.5	2E+07
	Vd = 16V Pout = 34.5dBm Pdiss = 5.5W	151	12.0	4E+06
	Vd = 20V Pout = 36.5dBm Pdiss = 8W	192	13.4	4E+05

(1) Assuming 85°C T_{case}.



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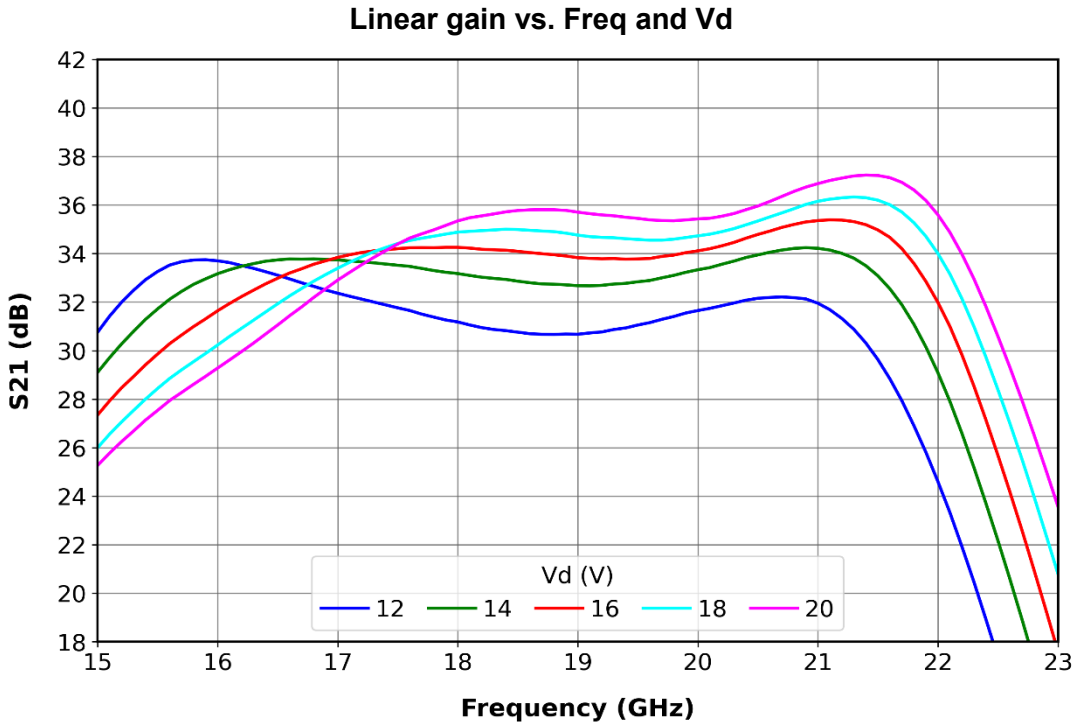
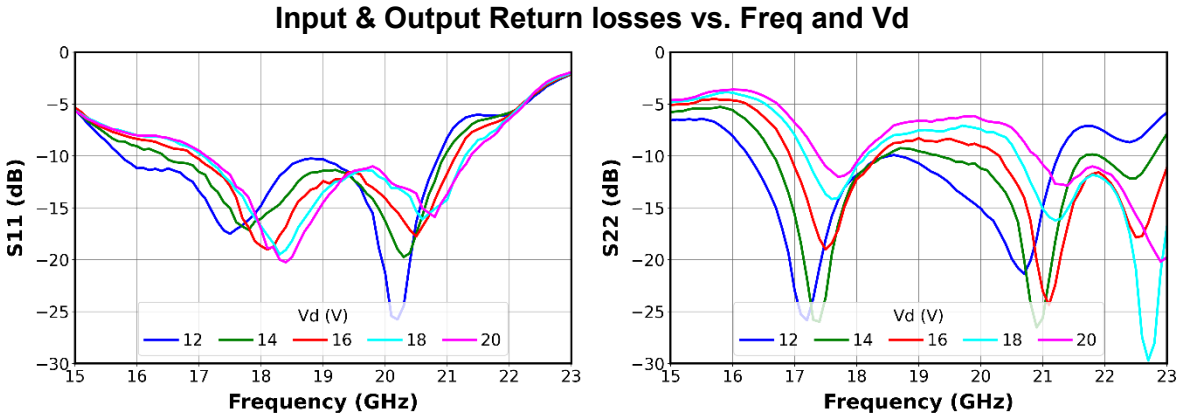
Typical Board Measurements

Board losses are de-embedded. Measurements are given in the package reference planes.
Test conditions : CW, T_{case} = 25°C, Idq = 125mA





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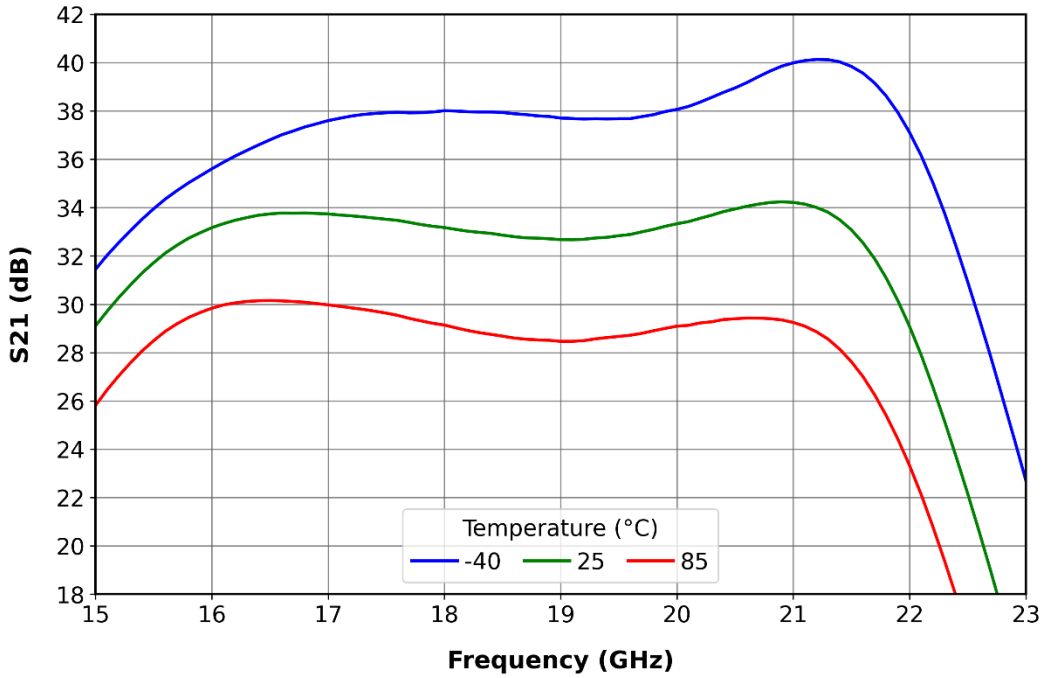
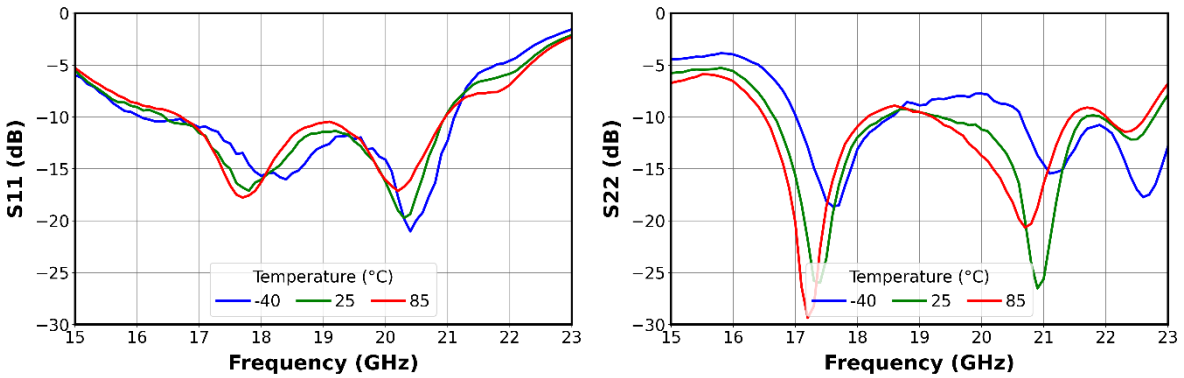
Linear gain vs. Freq and Temperature



Input & Output Return losses vs. Freq and Temperature



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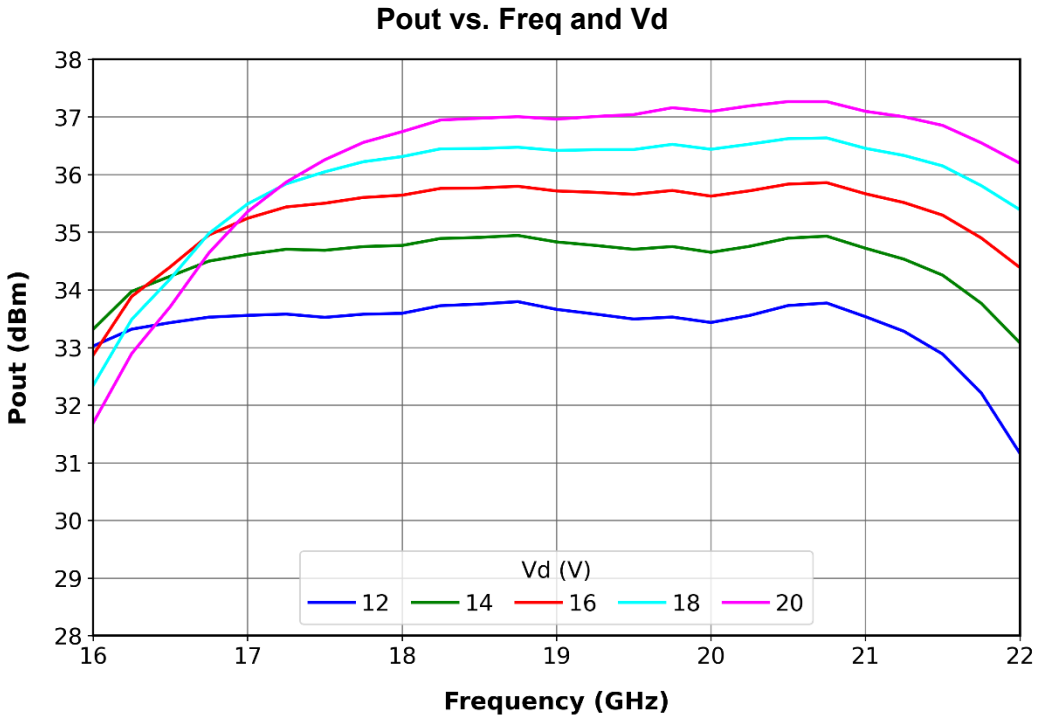
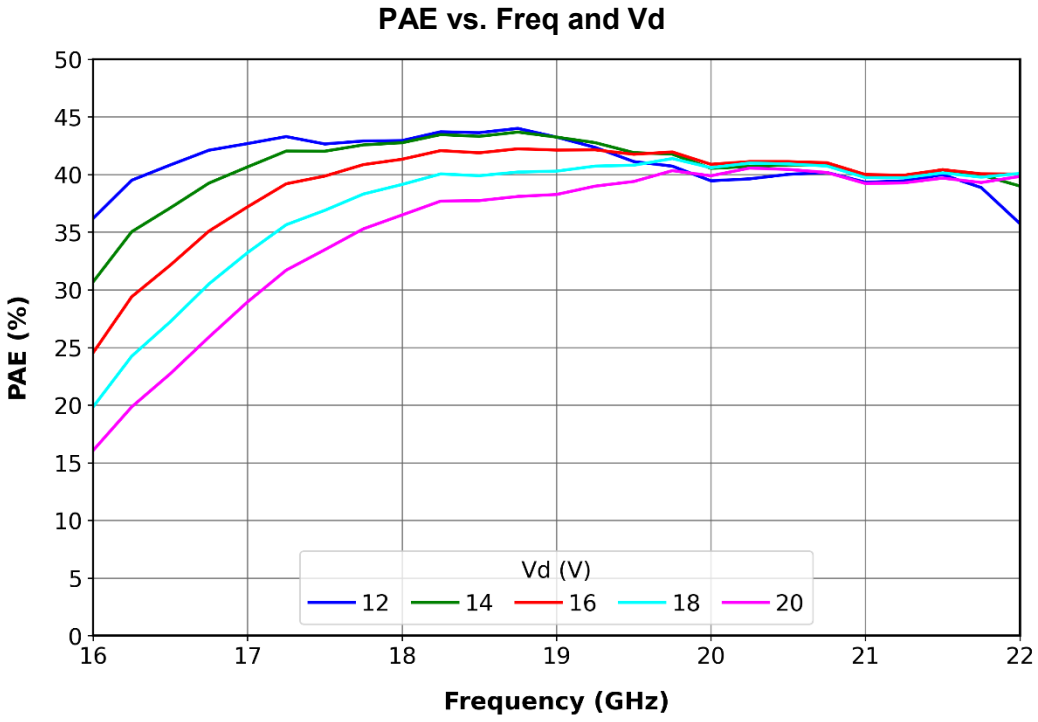
Test conditions : CW, T_{case} = 25°C, Idq = 125mA, Pin = 12dBm





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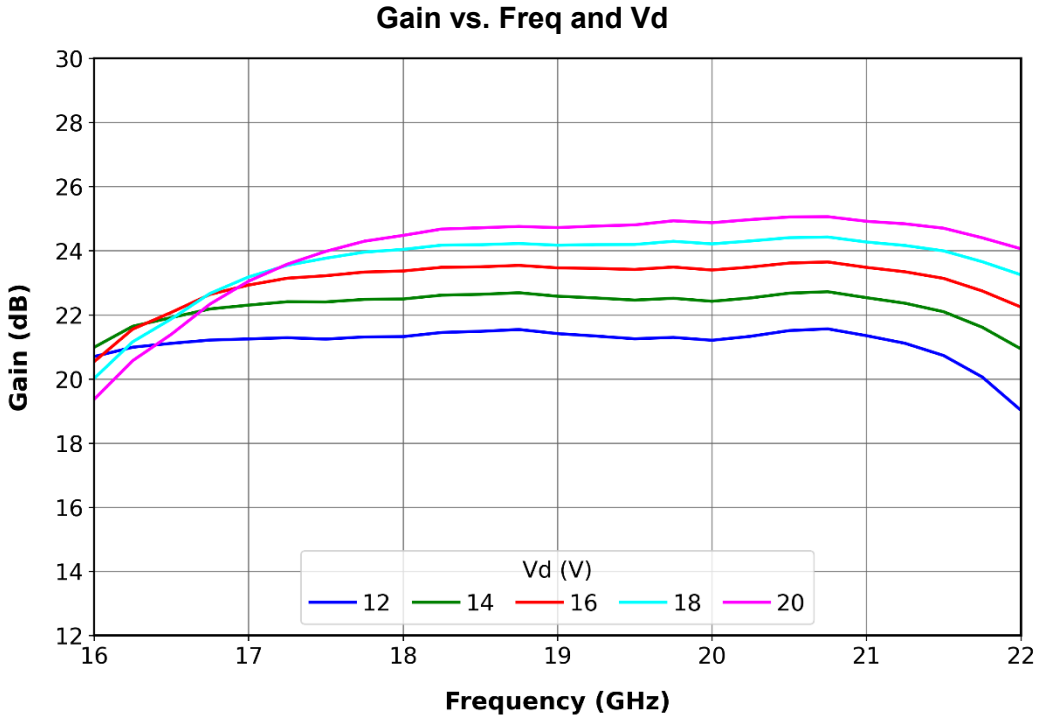

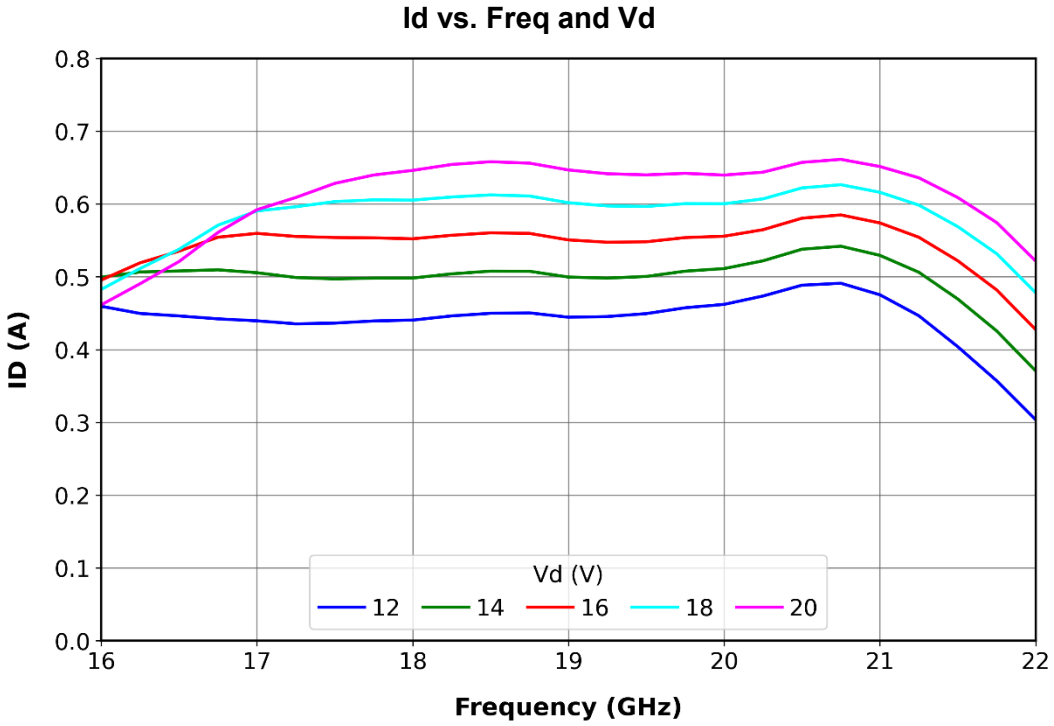

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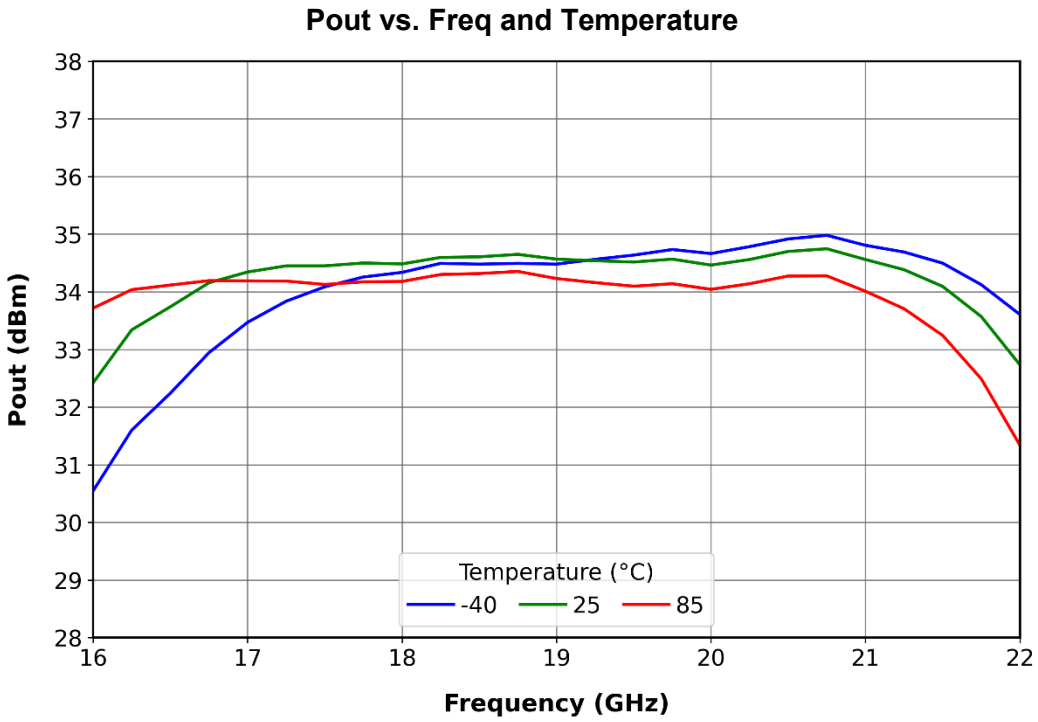
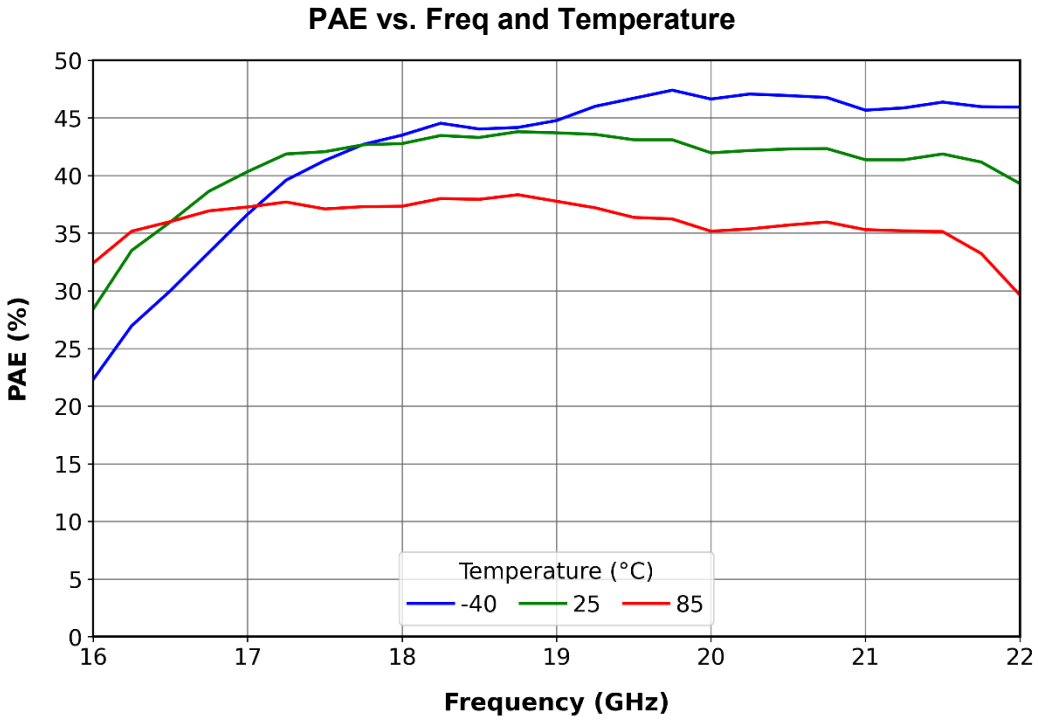
Test conditions : CW, Vd = 14V, Idq = 125mA
Pin = 6dBm@-40°C, Pin = 10dBm@25°C, Pin = 14dBm@85°C





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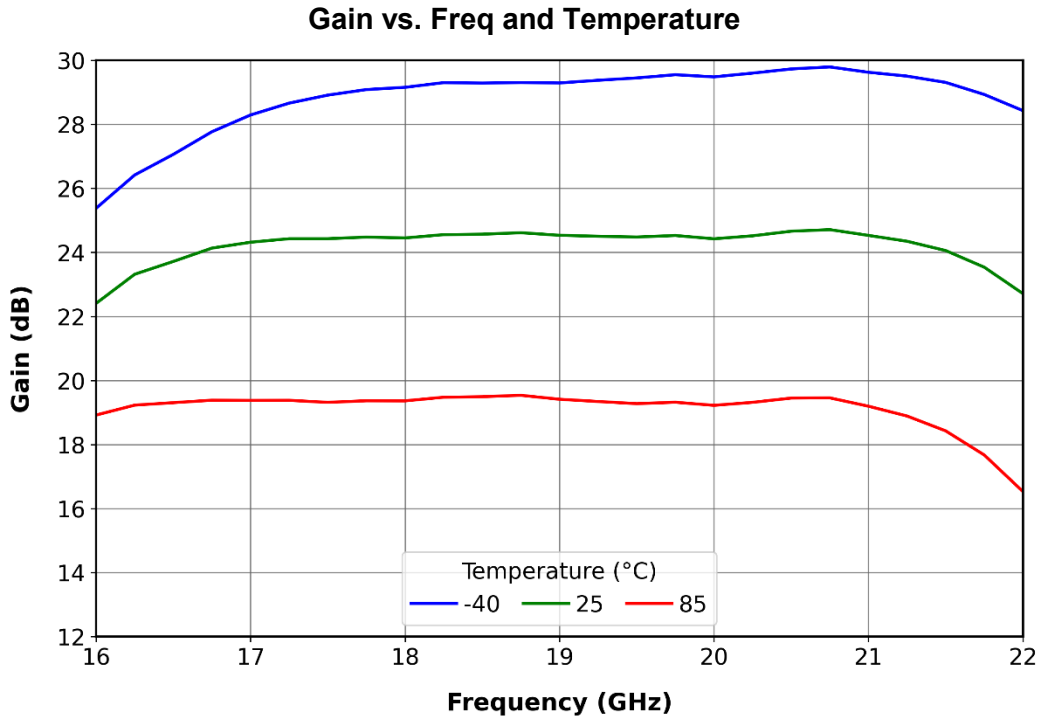

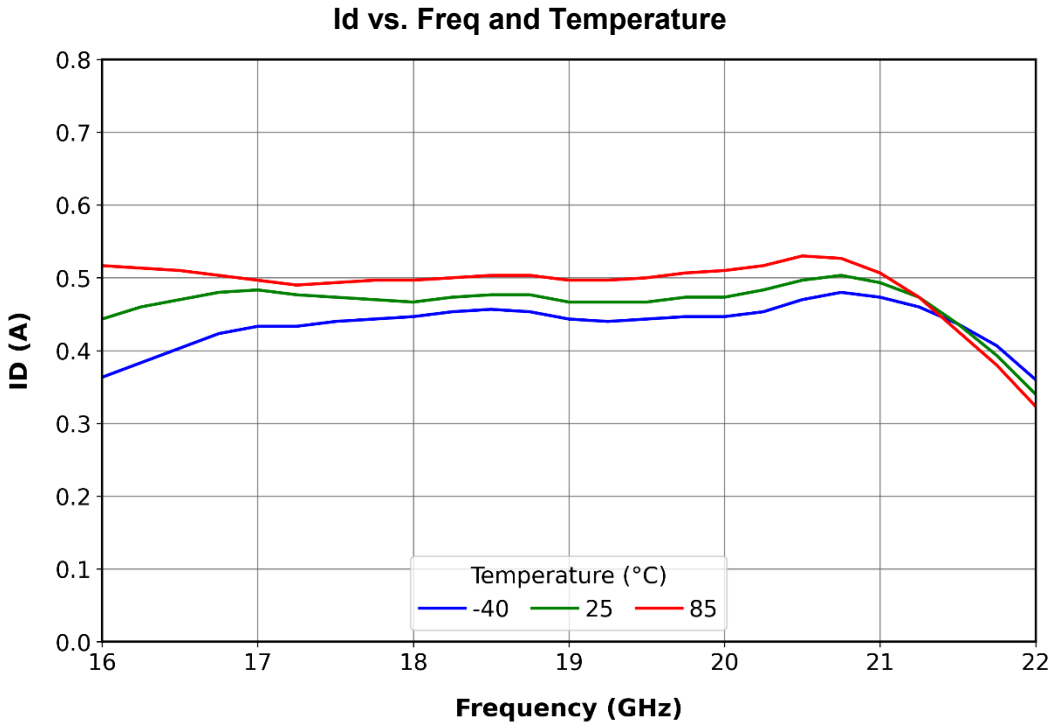

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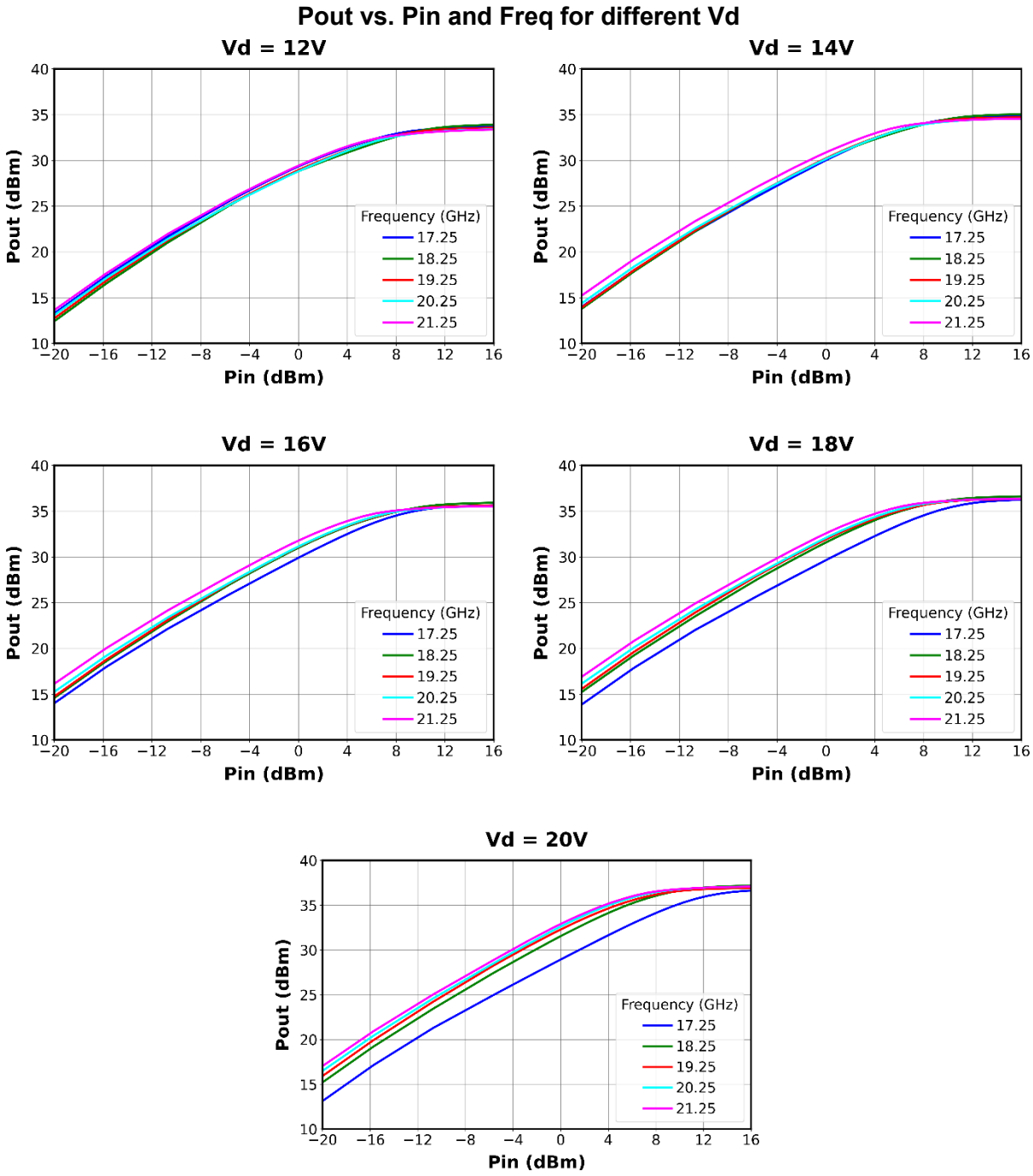

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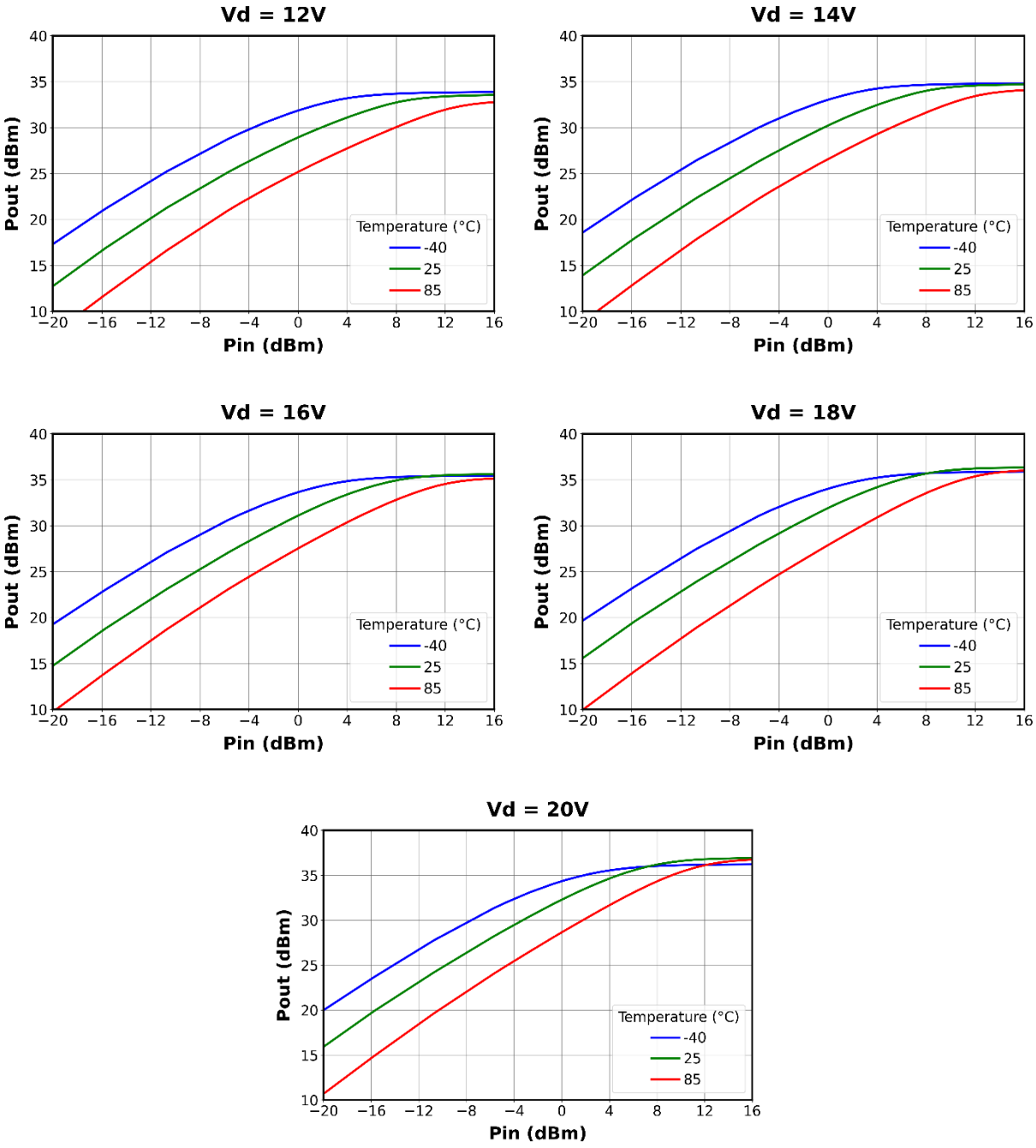
Typical Board Measurements

Board losses are de-embedded. Measurements are given in the package reference planes.
Test conditions : CW, Frequency = 19.25GHz, Idq = 125mA

Pout vs. Pin and Temperature for different Vd



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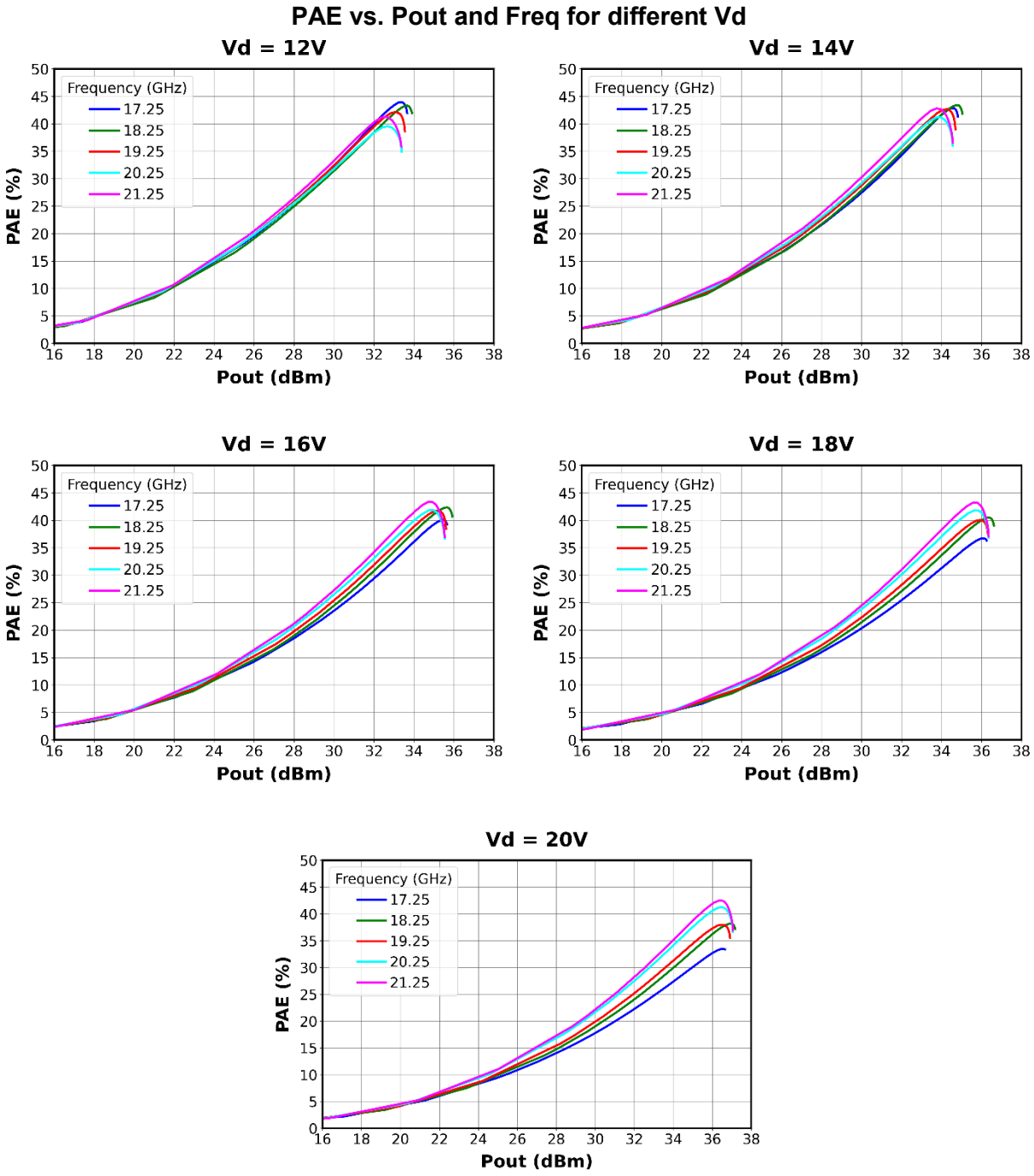

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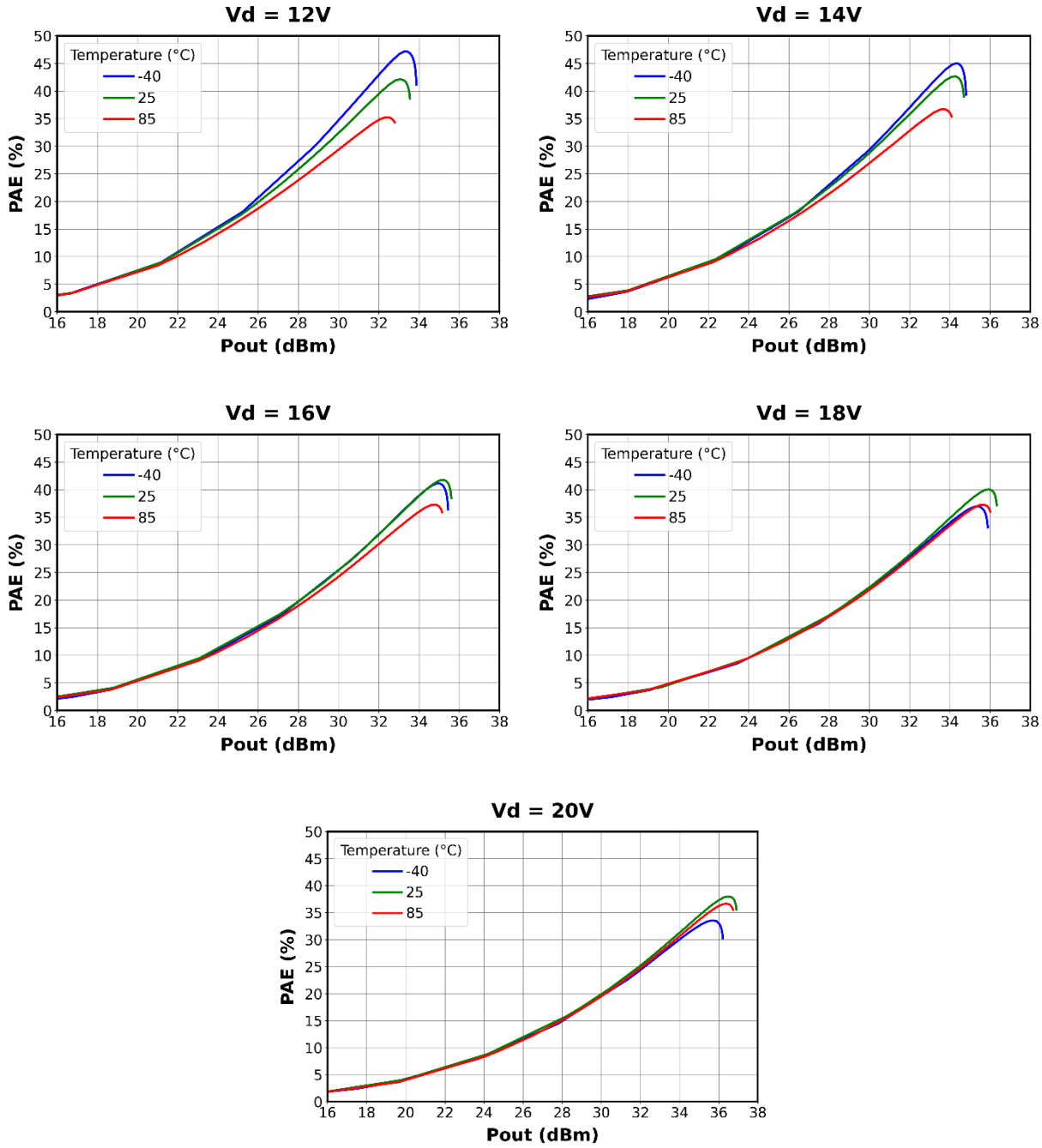
PAE vs. Pout and Temperature for different Vd



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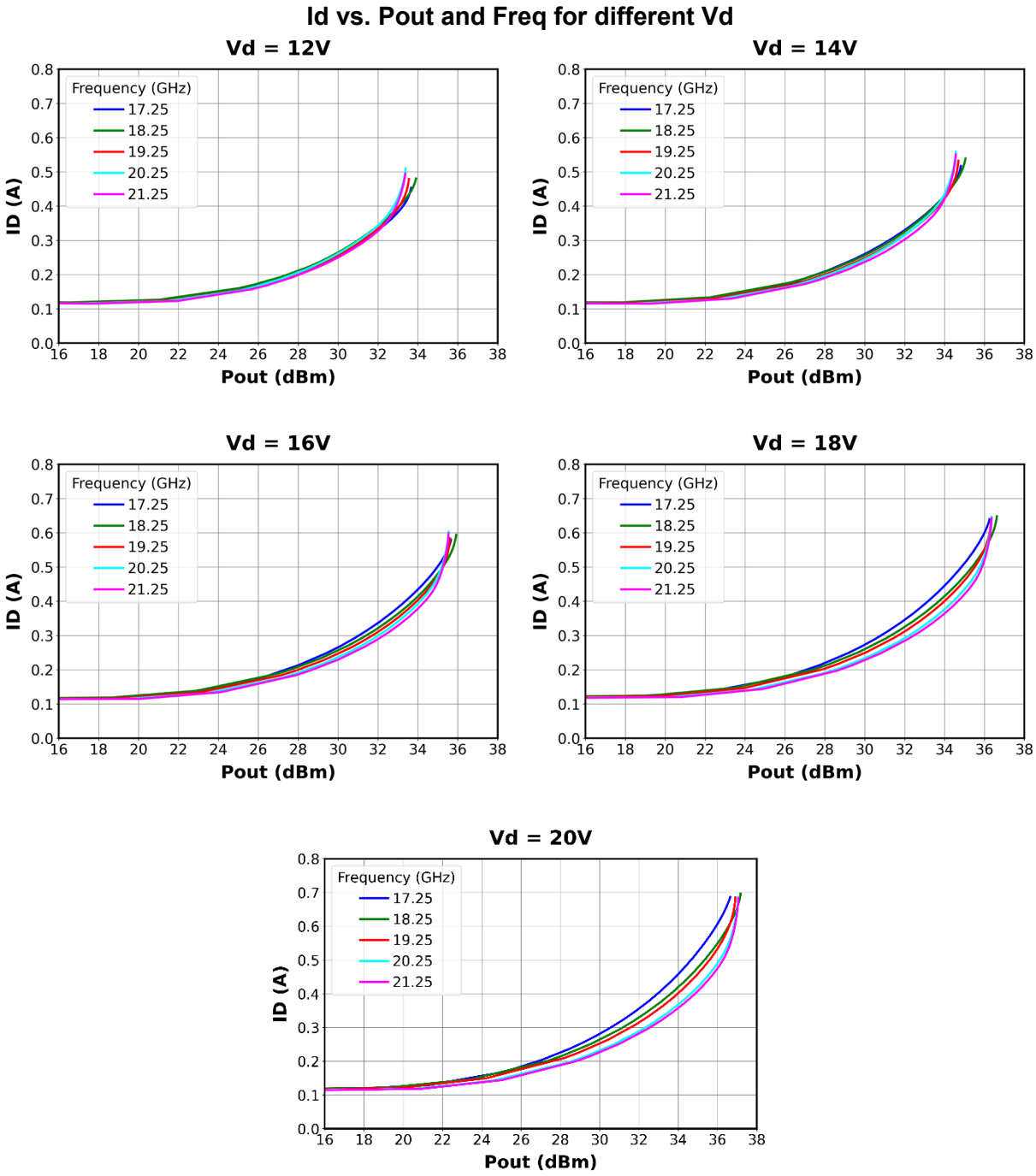

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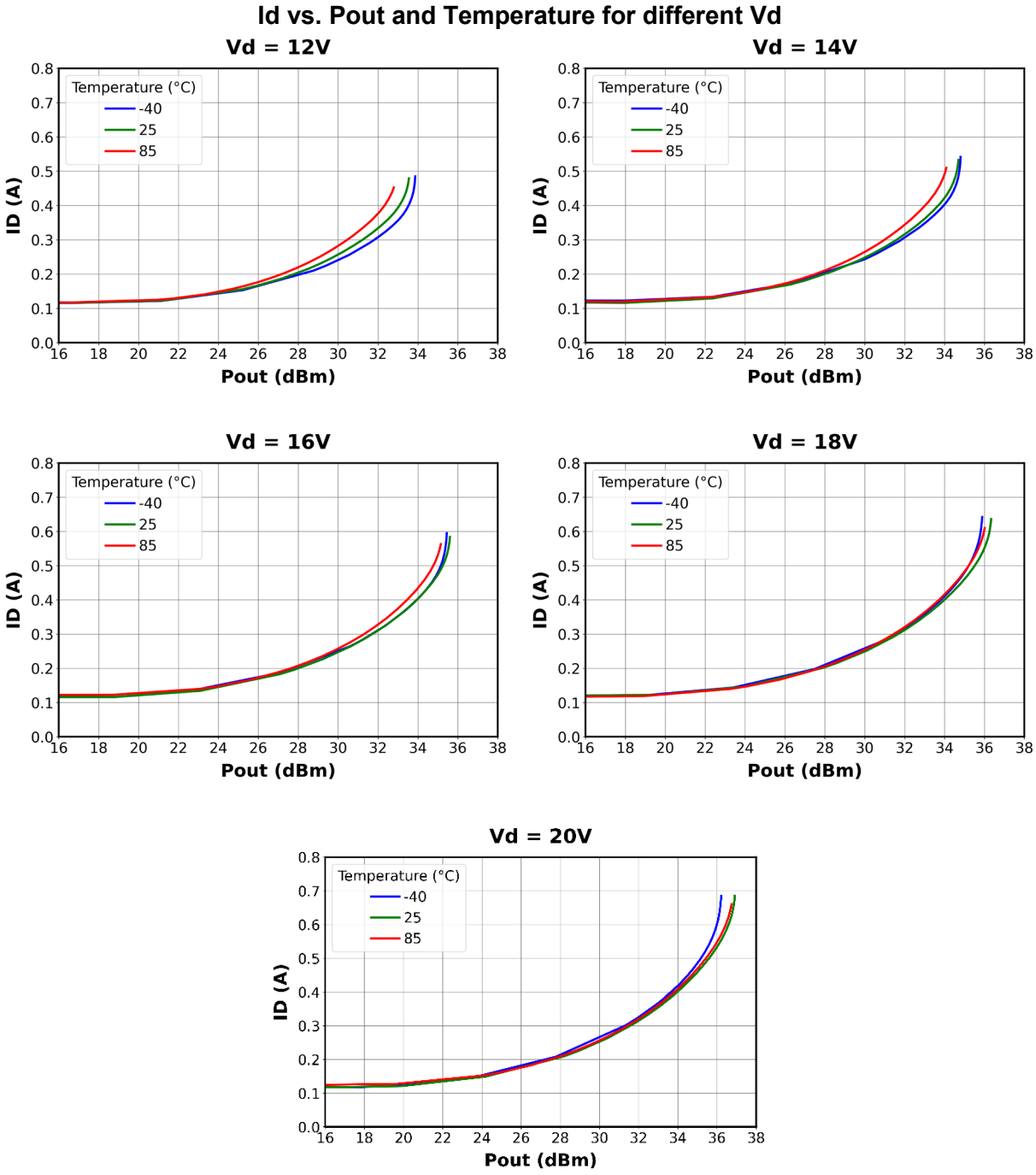
Test conditions : CW, Frequency = 19.25GHz, Idq = 125mA



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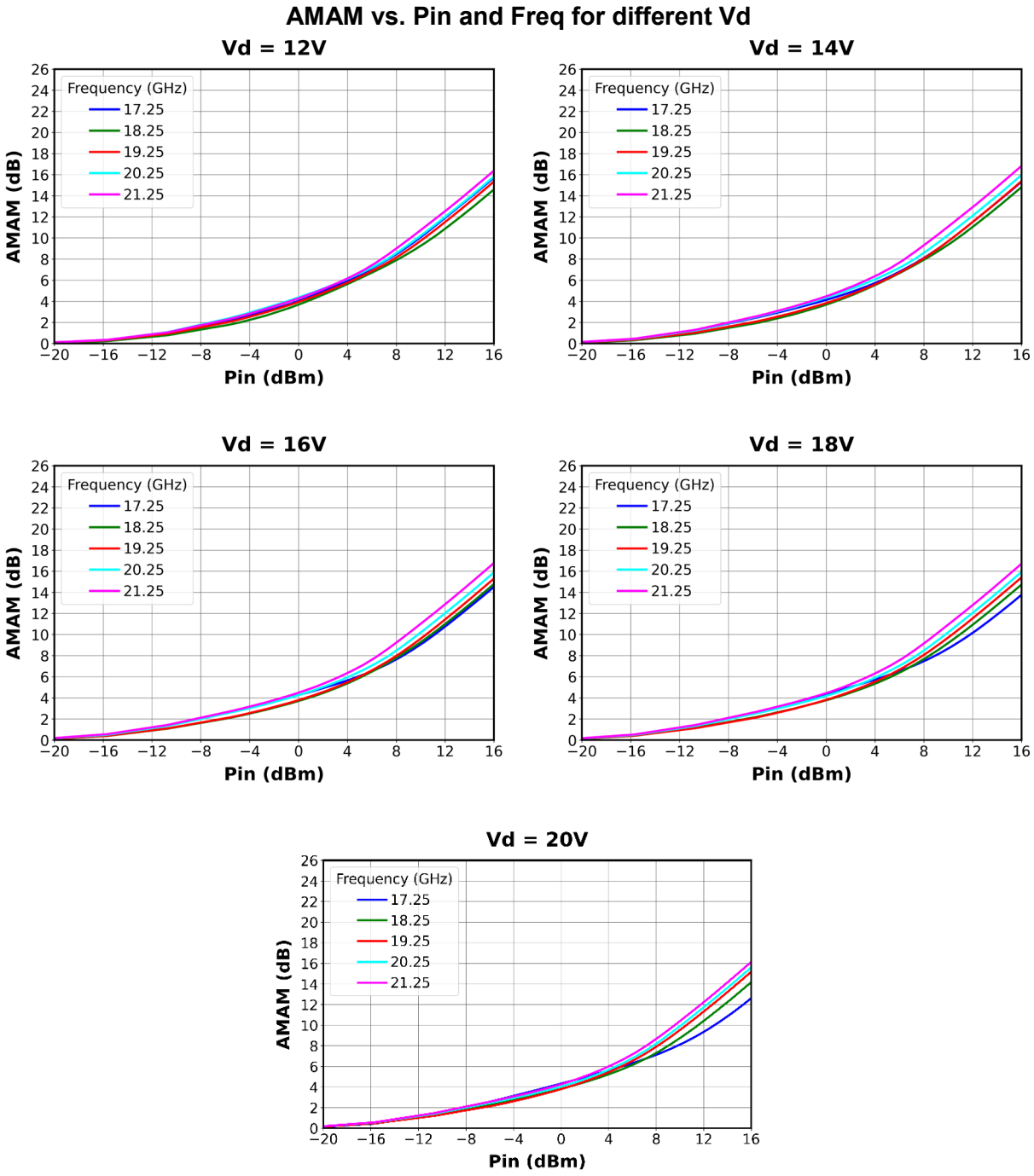

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Typical Board Measurements

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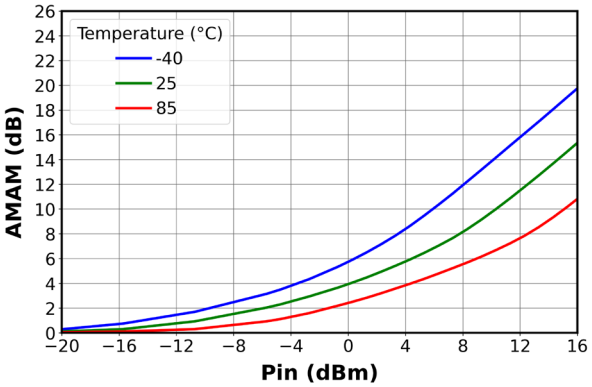
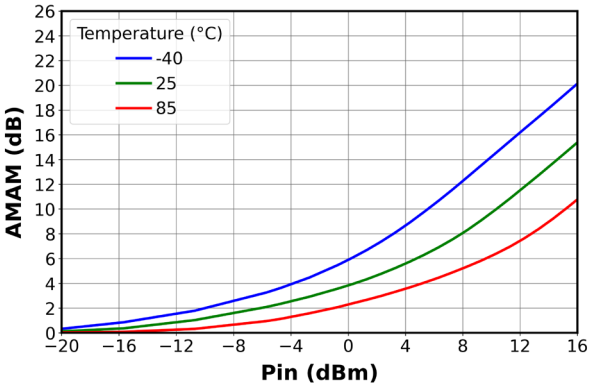
Test conditions : CW, Frequency = 19.25GHz, Idq = 125mA

AMAM vs. Pin and Temperature for different Vd

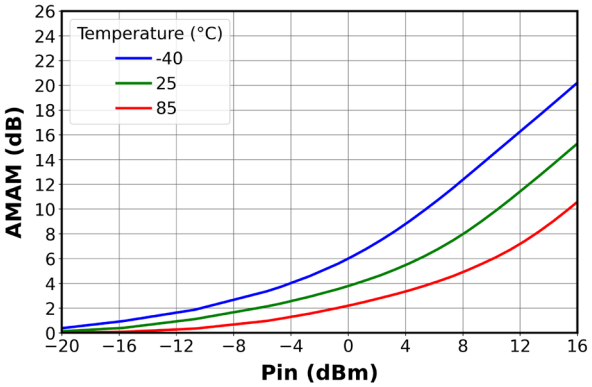
Vd = 12V



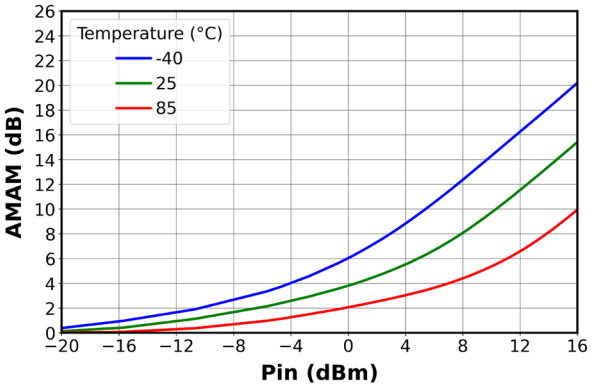
Vd = 14V



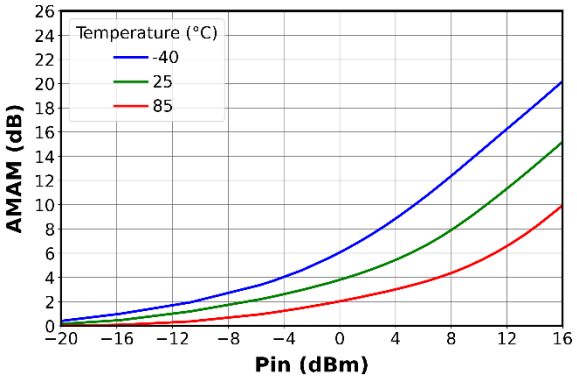
Vd = 16V



Vd = 18V



Vd = 20V



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Typical Board Measurements

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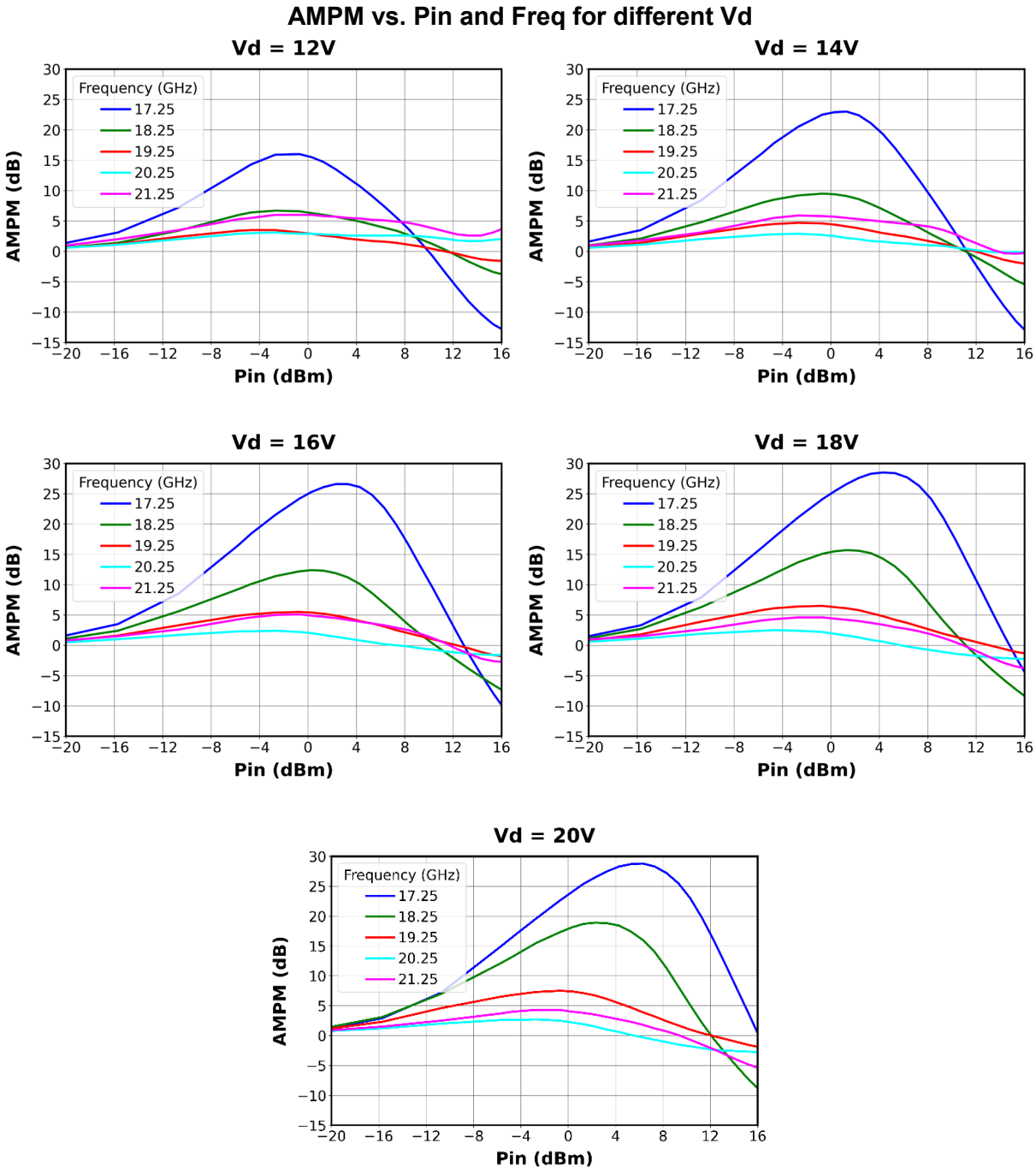
Test conditions : CW, T_{case} = 25°C, Idq = 125mA



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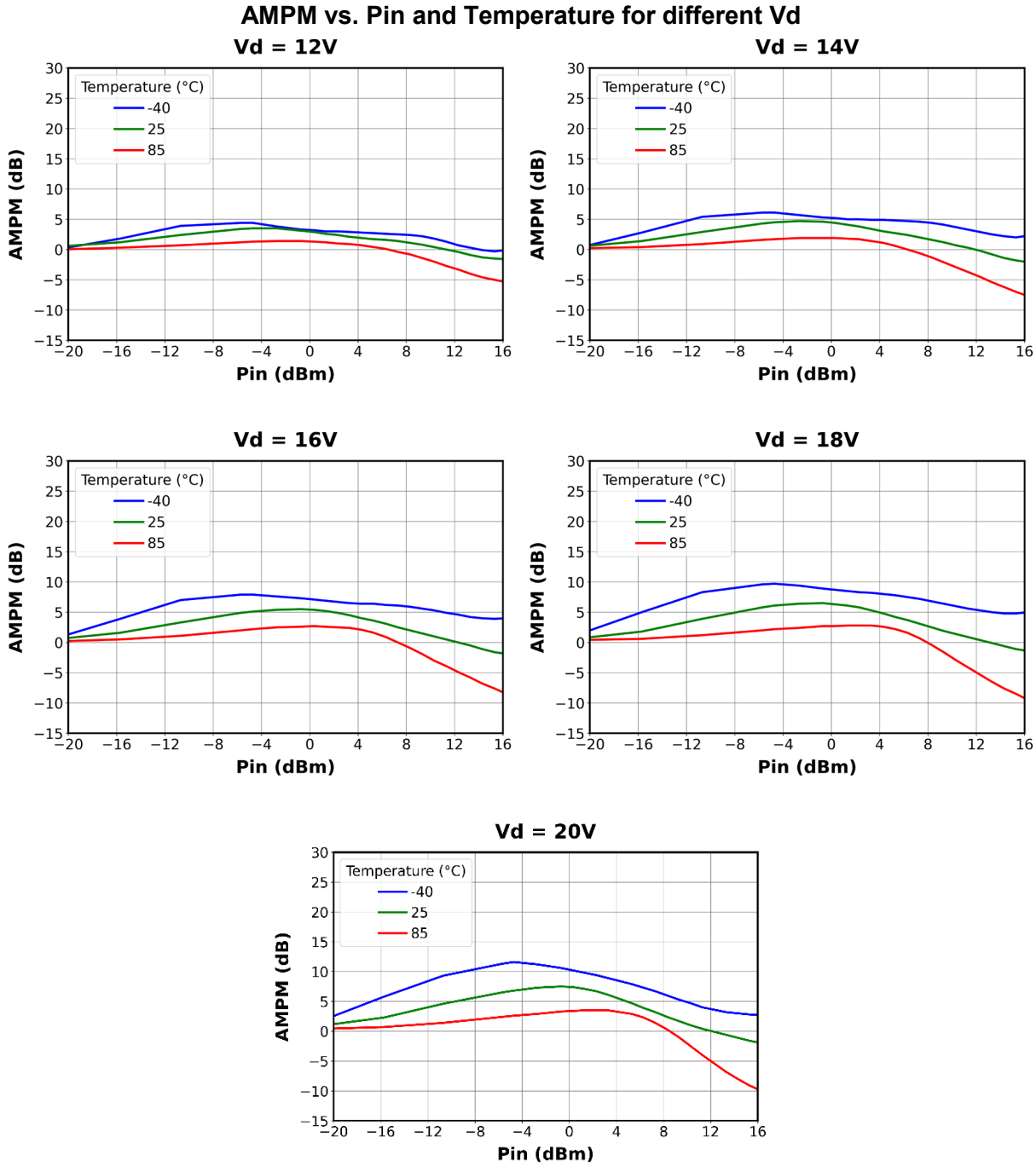

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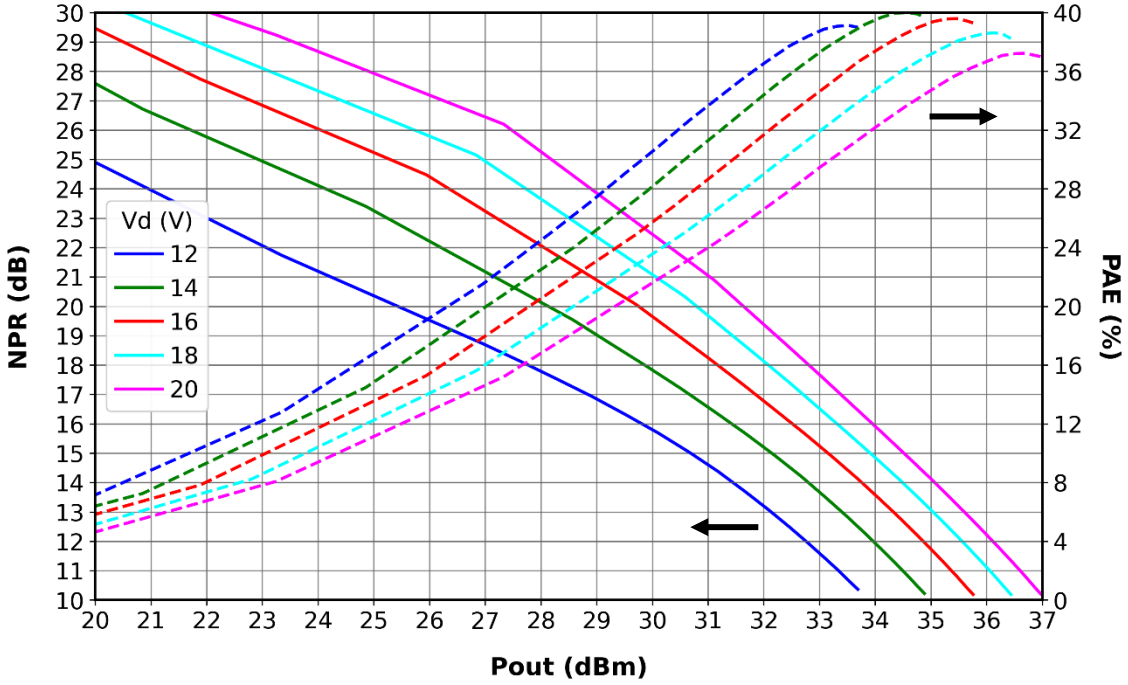
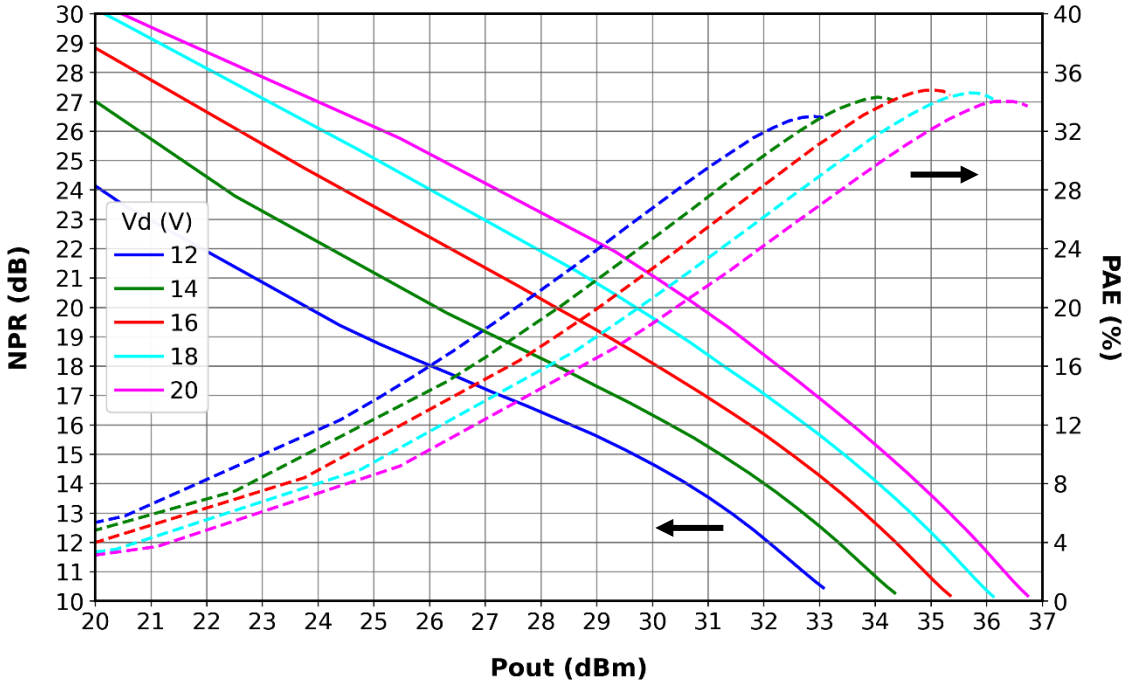
Typical Board Measurements

Board losses are de-embedded. Measurements are given in the package reference planes.
Test conditions : Idq = 125mA, Bandwidth = 1GHz, Center Freq = 19.45GHz, Notch = 10%

NPR & PAE vs. Pout and Vd for T_{case} = 25°C



NPR & PAE vs. Pout and Vd for T_{case} = 85°C



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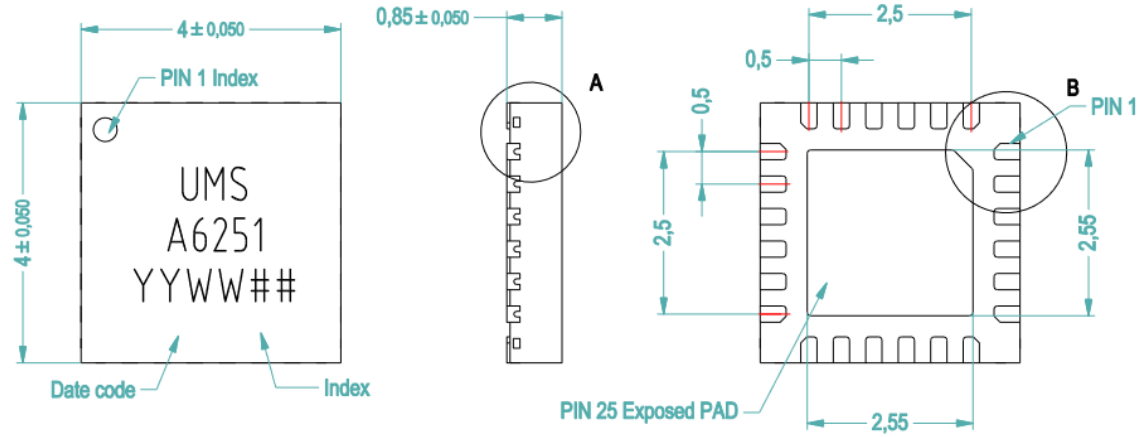
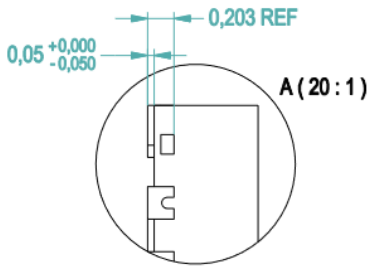
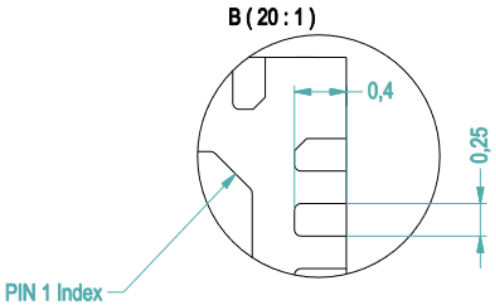
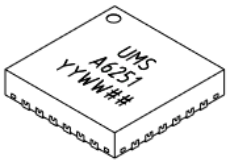
Package Outline







Units : mm
Finish : NiPdAuAg
Lead free (Green)



Units :	mm	1- NC	11- VG3	21- GND(1)
Finish :	NiPdAuAg	2- NC	12- NC	22- VD1
MSL Rating :	MSL3	3- GND(1)	13- NC	23- NC
Lead Free (Green)		4- RFin	14- GND(1)	24- NC
From the standard :	JEDEC MO-220 VGGD	5- GND(1)	15- RFout	25- GND(1)
		6- NC	16- GND(1)	
NC :	Not Connected	7- NC	17- NC	
		8- VG1	18- NC	
		9- GND(1)	19- VD3	
		10- VG2	20- VD2	

(1) It is strongly recommended to ground all pins marked “GND” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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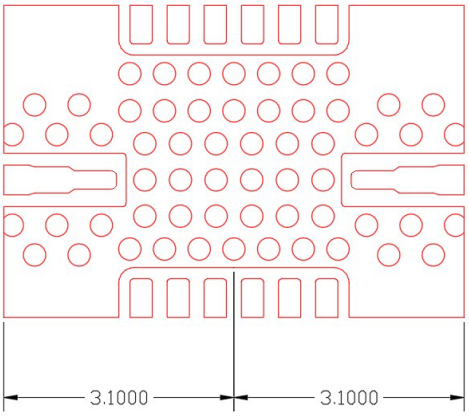
Definition of measurements reference planes

The reference planes used measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.1mm offset (input wise and output wise respectively) from this axis.



ESD sensitivity

Parameter	Classification	Standard
Human Body Model (HBM)	1A	ANSI/ESDA/JEDEC - JS-001

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	NiPdAuAg
MSL Rating	MSL3

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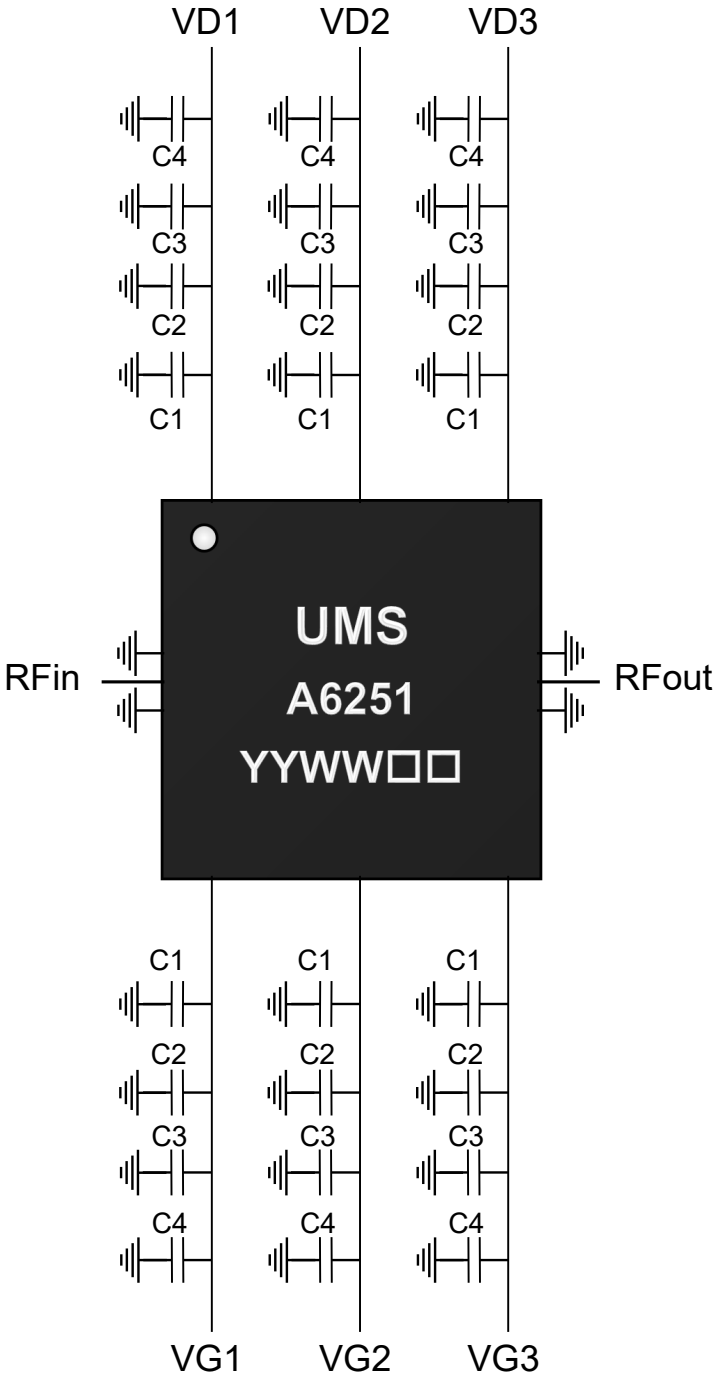
Recommended Assembly Plan



Bill of Materials

Label	Value	Description
C1	RF	Capacitor 120pF ±15% 50V
C2	RF	Capacitor 10nF ±10% 50V
C3	RF	Capacitor 1µF ±10% 50V
C4	RF	Capacitor 10µF ±10% 50V

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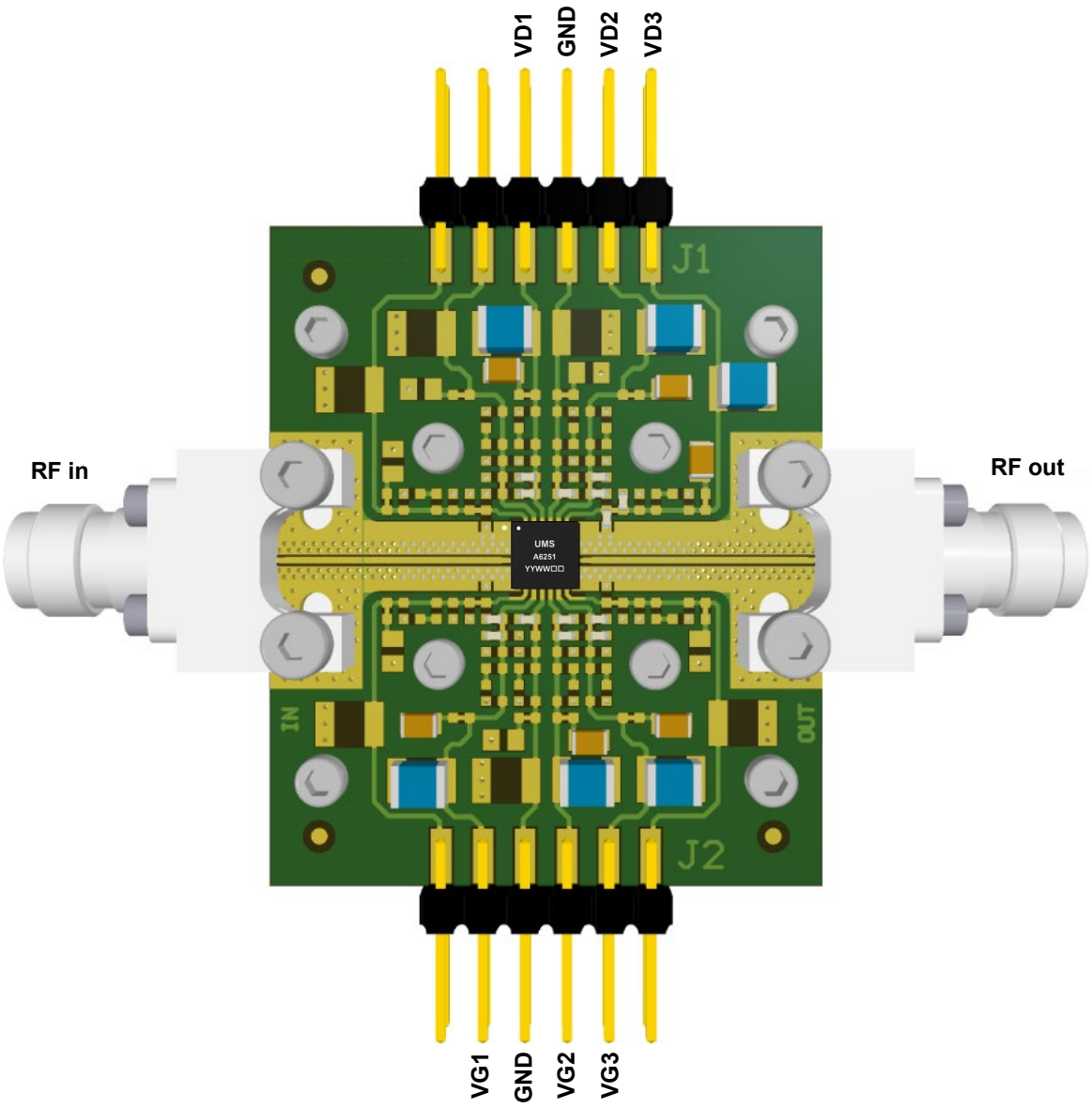
Evaluation Board

- Compatible with the proposed footprint.
- Based on typically Ro4350 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 120pF, 10nF, 1µF, 10µF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Description of Evaluation Board

Refer to the application note AN0031 available at https://www.ums-rf.com for the description of Evaluation Board for Packaged Die and recommendations for this UMS package product.

Ordering Information

QFN 4x4 package:	CHA6251-QKB/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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