United Monolithic Semiconductors

CHA8254-99F

10W K-Band Doherty Power Amplifier

GaN Monolithic Microwave IC

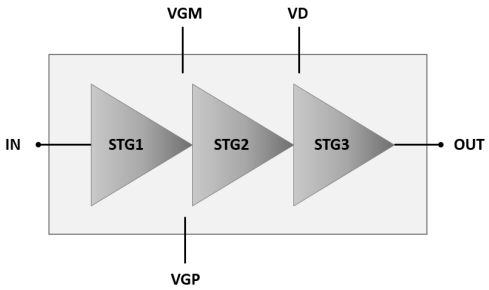
Description

The CHA8254-99F is a three-stage GaN Doherty Power Amplifier in the frequency band 17.3-20.3GHz. This DPA typically provides 10W of output power associated to 31% of Power Added Efficiency. Thanks to Doherty architecture, it also provides 27% Power Added Efficiency at 6dB of input back-off. The small signal gain reaches more than 29dB. The overall power supply is 15V/210mA (quiescent current). Due to a low drain voltage biasing, the CHA8254-99F provides a junction temperature below 160°C even in saturation.

This circuit is a very versatile amplifier for high performance systems.

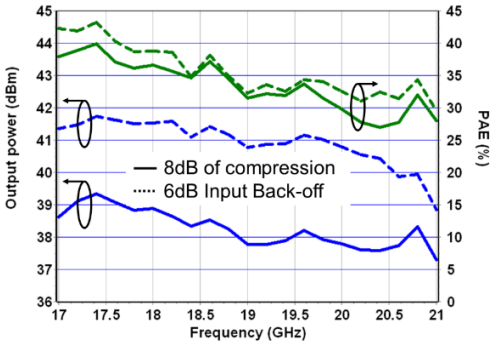
The circuit is firstly dedicated to space applications and well suited for a wide range of microwave applications and systems.

The part is developed on a robust GaN on SiC HEMT process and is available as a bare die.



Main Features

- 17.3-20.3 GHz frequency range
- Linear Gain is 29dB
- 40dBm Pout for +20dBm input power
- Associated PAE is more than 31% for +20dBm input power and 27% for +14dBm input power
- DC bias: Vd=15Volts @Idq_main=210mA @Idq_peak=15mA
- Chip size : 5x3.6x0.07mm



Main Electrical Characteristics

$T_{backside}$= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.3		20.3	GHz
Gain	Linear Gain		29		dB
PAE	Power Added Efficiency at 6dB Input Back-off (Pin=14dBm)		27		%
Pout	Output Power (Pin=20dBm)		40		dBm

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Specifications (CW mode)

$T_{backside}$= +25°C, Vd = +15V, Idq_Main (VGM) = 210mA, Idq_Peak (VGP)=15mA,

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.3		20.3	GHz
Gain	Linear Gain		29		dB
Pout	Output Power (Pin = 20dBm)		40		dBm
PAE	Associated Power Added Efficiency (Pin = 20dBm)		31		%
PAE	Power Added Efficiency at 6dB Input Back-Off (Pin = 14dBm)		27		%
Id	Drain current at saturation (Pin = 20dBm)		2.2		A
S11	Input Return Loss		17		dB
S22	Output Return Loss		12		dB
Idq	Quiescent Current		0.21		A
Vd	Drain Voltage		15		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

Recommended Operating Ratings

$T_{backside}$= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	15V	V
Id_main_ stg_1_2_3	1st, 2nd and 3rd stage Main drain current (North) (2)	1.1	A
Id_peak_ stg_1_2_3	1st, 2nd and 3rd stage Peak drain current (South) (2)	1.1	A
Pin	Maximum peak input power overdrive	22	dBm
Tj	Maximum Junction temperature (1)	160	°C

(1) Value is provided for $T_{backside}$=85°C

(2) Currents are provided at saturation (with RF signal)

Absolute Maximum Ratings (3)

$T_{backside}$= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	25	V
Id_main_ stg_1_2_3	1st, 2nd and 3rd stage Main drain current (North) (2)	1.4	A
Id_peak_ stg_1_2_3	1st, 2nd and 3rd stage Peak drain current (South) (2)	1.4	A
Pin	Maximum peak input power overdrive	25	dBm

(3) Operation of this device above anyone of these parameters may cause permanent damage.

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Temperature Range

$T_{backside}$	Operating temperature range (chip backside temperature reference)	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

$T_{backside}$= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
Vg_main	2,6,10	Gate voltage tuned for Idq ~ 210mA	-3	V
Vg_peak	16,20,24	Gate voltage tuned for Idq ~ 15mA	-3.4	V
Vd	4,8,12,14,18,22	Drain Voltage	15	V

“Power ON” sequence

1. Bias HPA gate voltages at Vg close to Vpinch-off (example: Vg_main=Vg_peak≈ -5V).
2. Apply Vd bias voltage (example: Vd = 15V).
3. Increase slowly Vg_main up to quiescent bias drain current Ids0 (applied on the gate: 210mA).
4. Increase slowly Vg_peak up to quiescent bias drain current Ids0 (applied on the gate: 15mA).
5. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Bias HPA gate voltages at Vg close to Vpinch-off (example: Vg_main=Vg_peak≈ -5V).
3. Set Vd to 0V.
4. Turn off Vd supply.
5. Turn off Vg supply.

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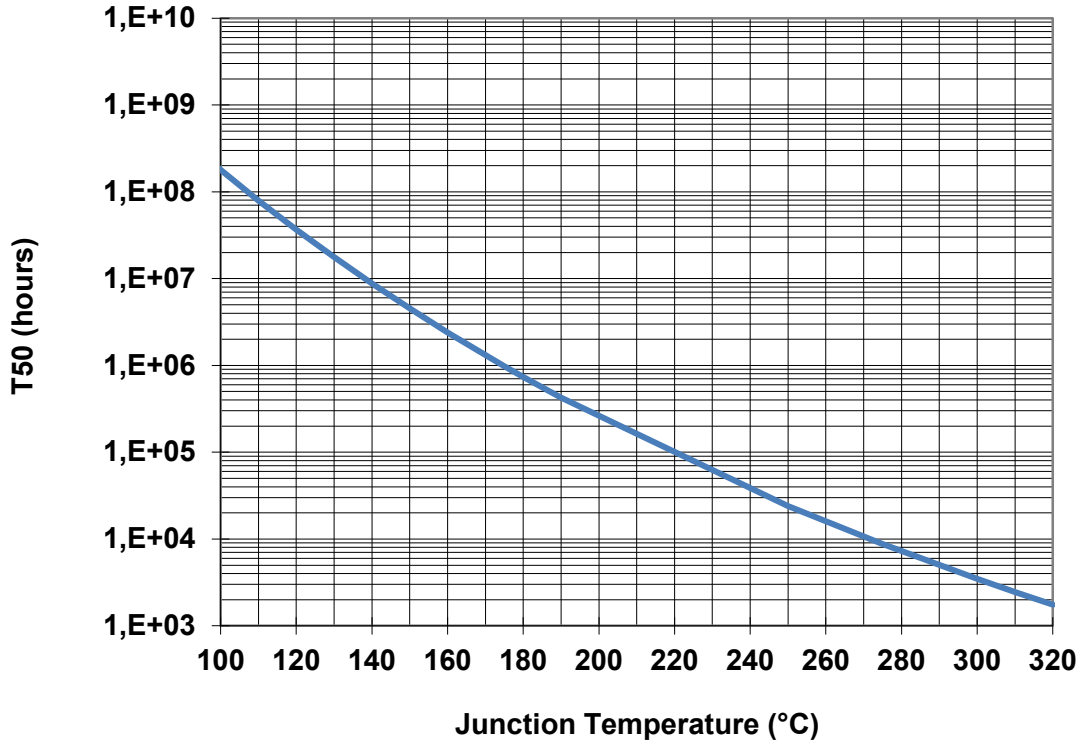
Device thermal information

The device thermal information below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA8254-99F is manufactured (GaN HEMT 0.15µm).
The temperature $T_{backside}$ is defined as the chip backside temperature. The thermal resistance (Rth_eq), given in the following table, is for the full circuit in CW mode.

Thermal Resistance(1)	Rth_eq	$T_{backside}$ = 85°C, Vd = 15V, Id_drive =1.1A Pin = 14dBm, Pout = 37dBm Pdiss = 13W CW	2.6	°C/W
Junction Temperature	Tj		120	°C
Median Life	T50		3.5E07	Hrs

(1) Thermal resistance measured at the back of the chip

Median Life Time vs. Junction Temperature



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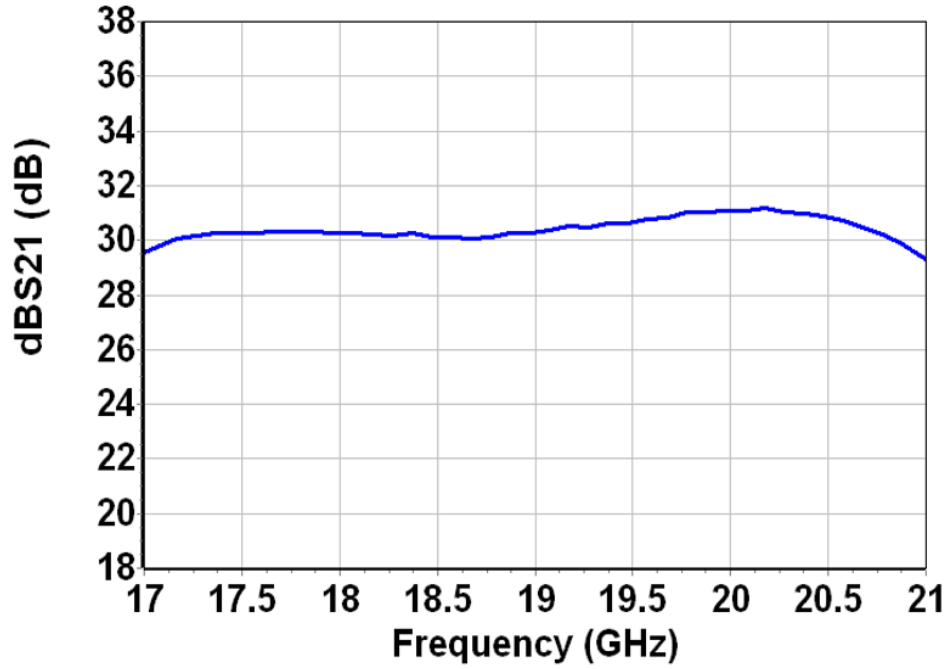
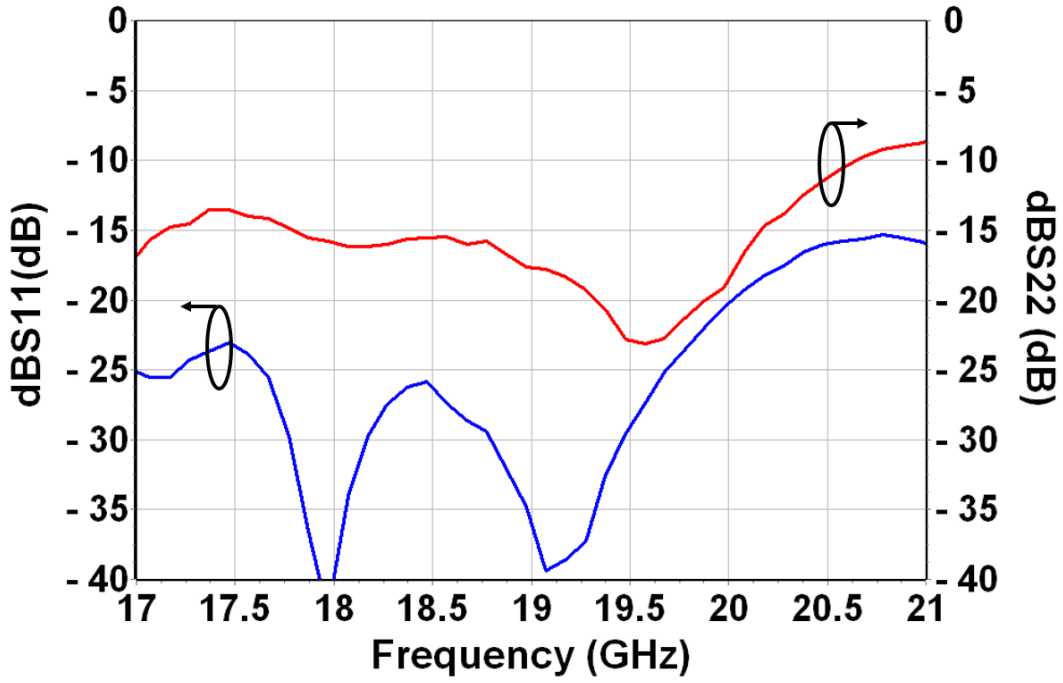
Typical Test Fixture Measurements: Small Signal Performances

CW measurements: $T_{backside}$= 25°C, Vd = +15V, Idq_Main (VGM) = 210mA, Idq_Peak (VGP)=15mA

Linear Gain vs. Frequency



Input and Output Return Loss vs. Frequency



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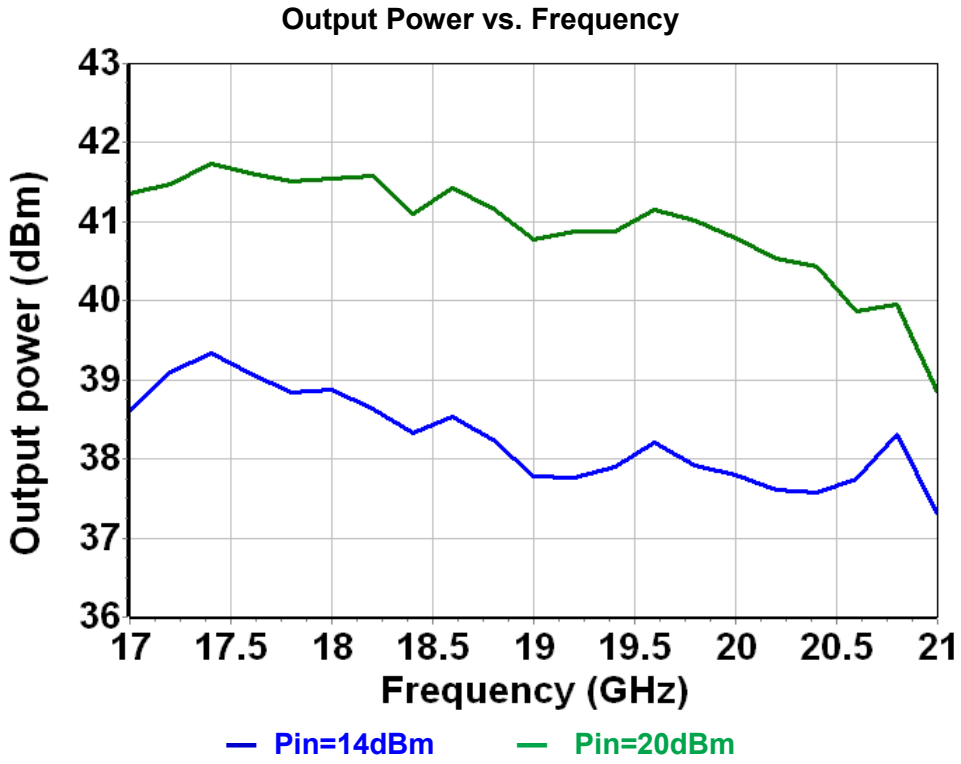
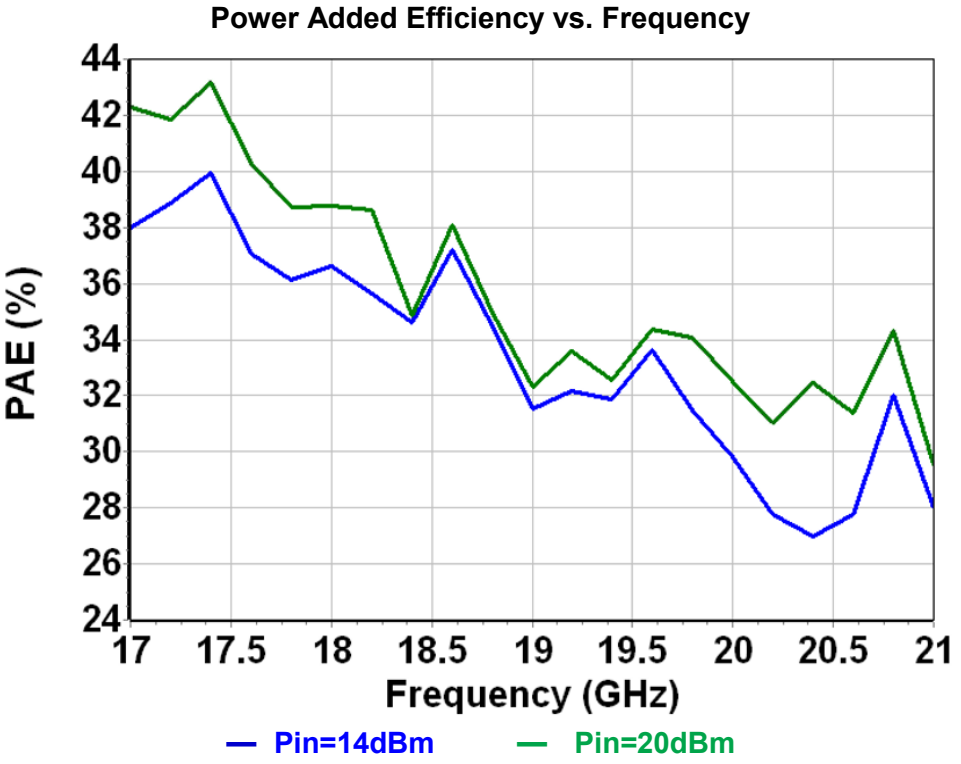
Typical Test Fixture Measurements: Non-linear performances

CW measurements: $T_{backside}$= 25°C, Vd = +15V, Idq_Main (VGM) = 210mA, Idq_Peak (VGP)=15mA
Pin: 14 or 20dBm, Frequency range: 17-21GHz step 0.2GHz





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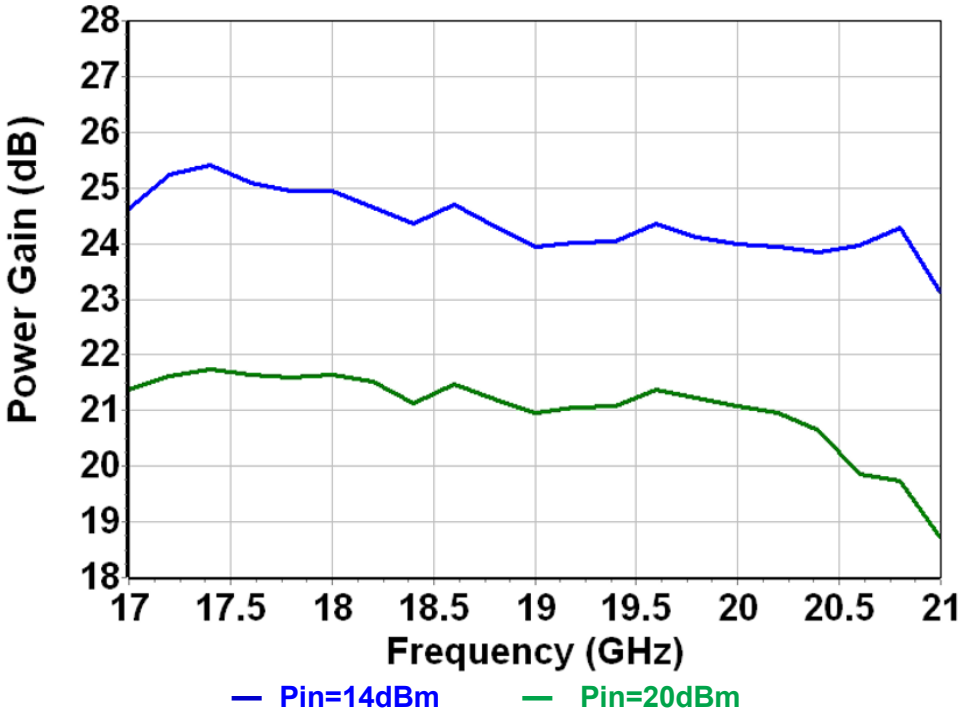
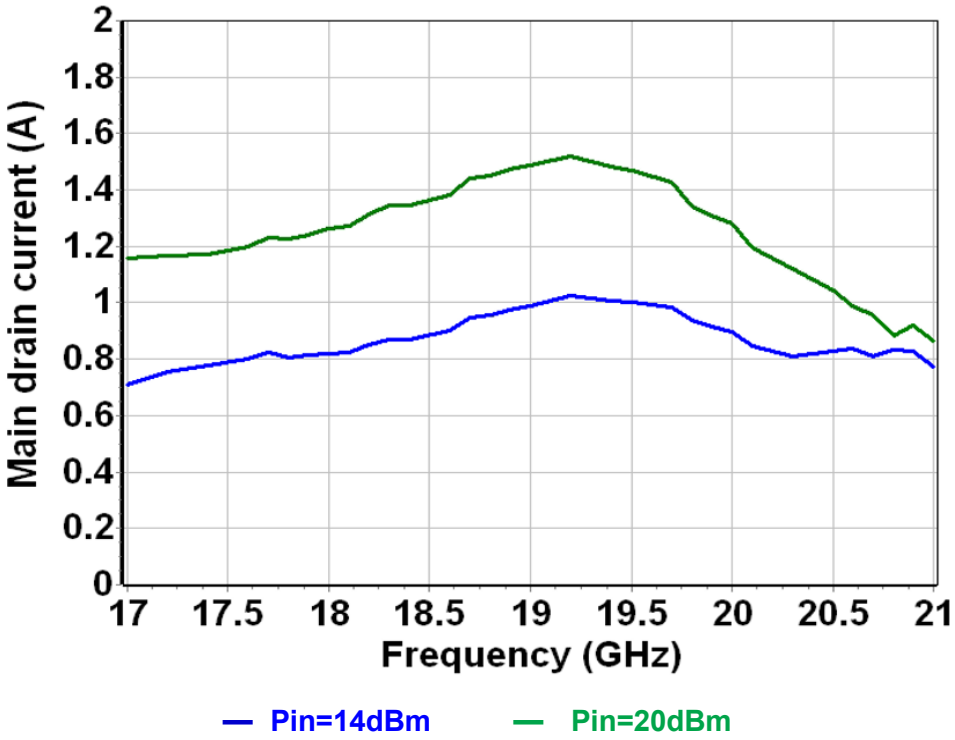
Pin: 14 or 20dBm, Frequency range: 17-21GHz step 0.2GHz

Power Gain vs. Frequency



Main Drain current (North) vs. Frequency



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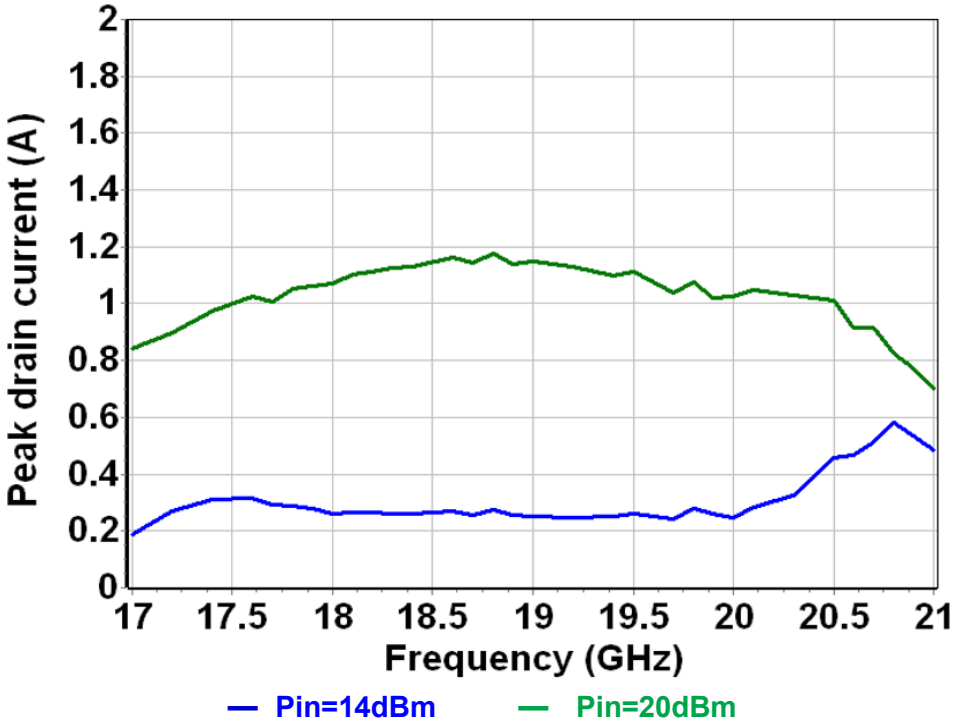
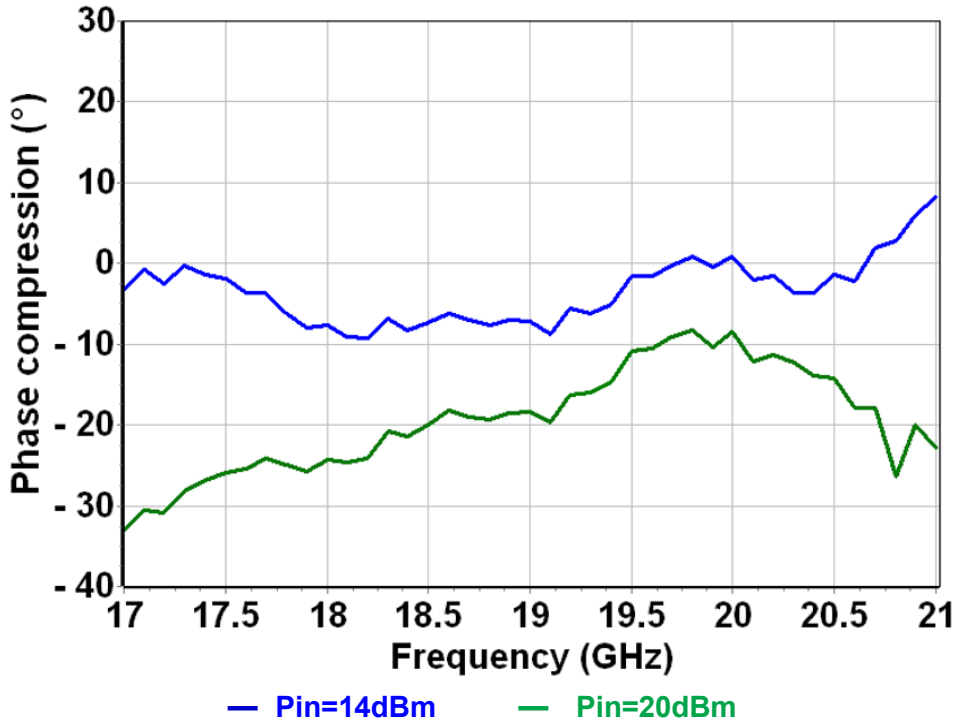
Typical Test Fixture Measurements: Non-linear performances

CW measurements: $T_{backside}$= 25°C, Vd = +15V, Idq_Main (VGM) = 210mA, Idq_Peak (VGP)=15mA
Pin: 14 or 20dBm, Frequency range: 17-21GHz step 0.2GHz

Peak Drain current (South) vs. Frequency



Phase compression vs. Frequency



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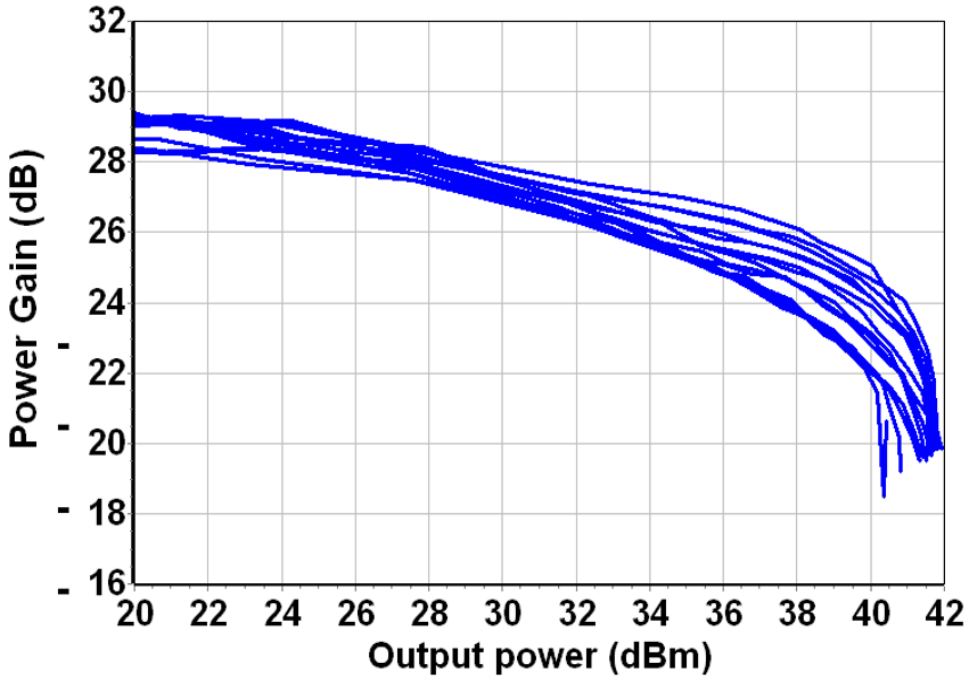
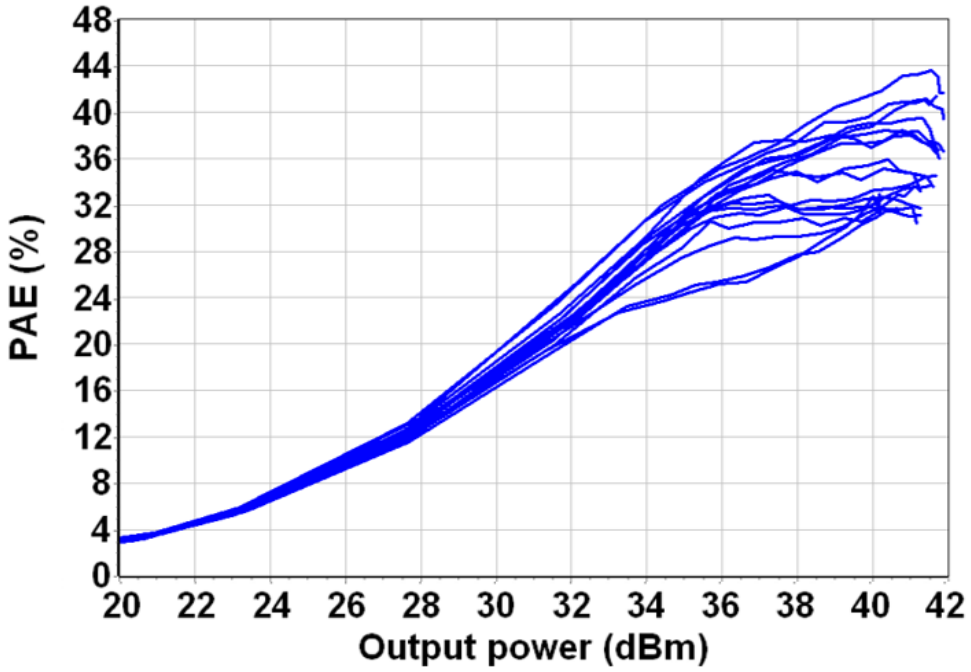
Typical Test Fixture Measurements: Non-linear Performances

CW measurements: $T_{backside}$= 25°C, Vd = +15V, Idq_Main (VGM) = 210mA, Idq_Peak (VGP)=15mA
Pin range : -15 to 20 dBm, Frequency range: 17.2-20.4 GHz step 0.2 GHz

Power Gain vs. Output power



PAE vs. Output power



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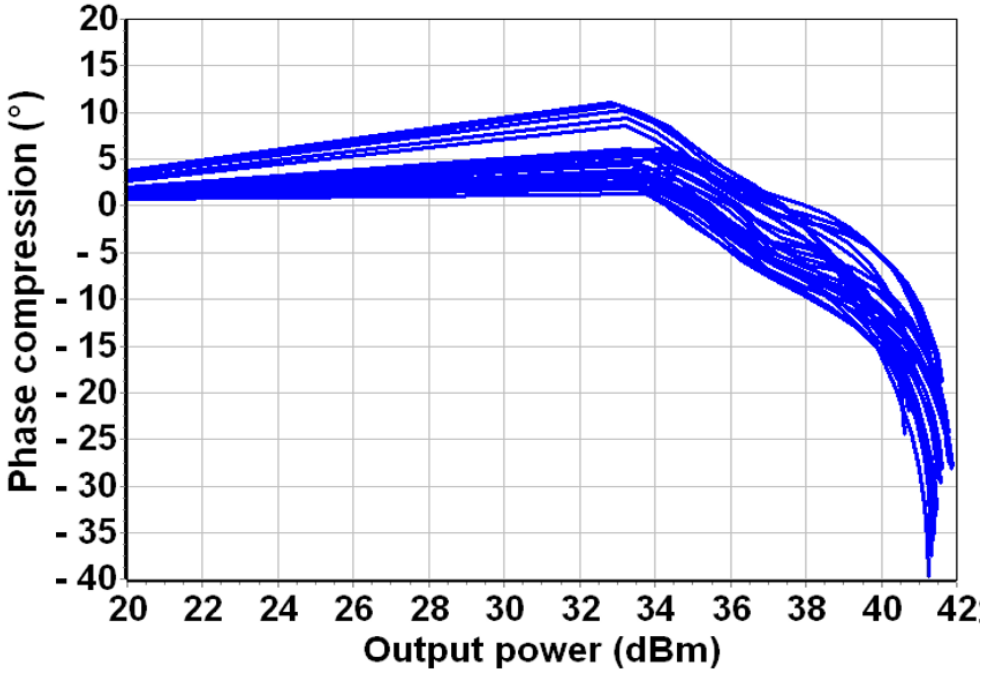
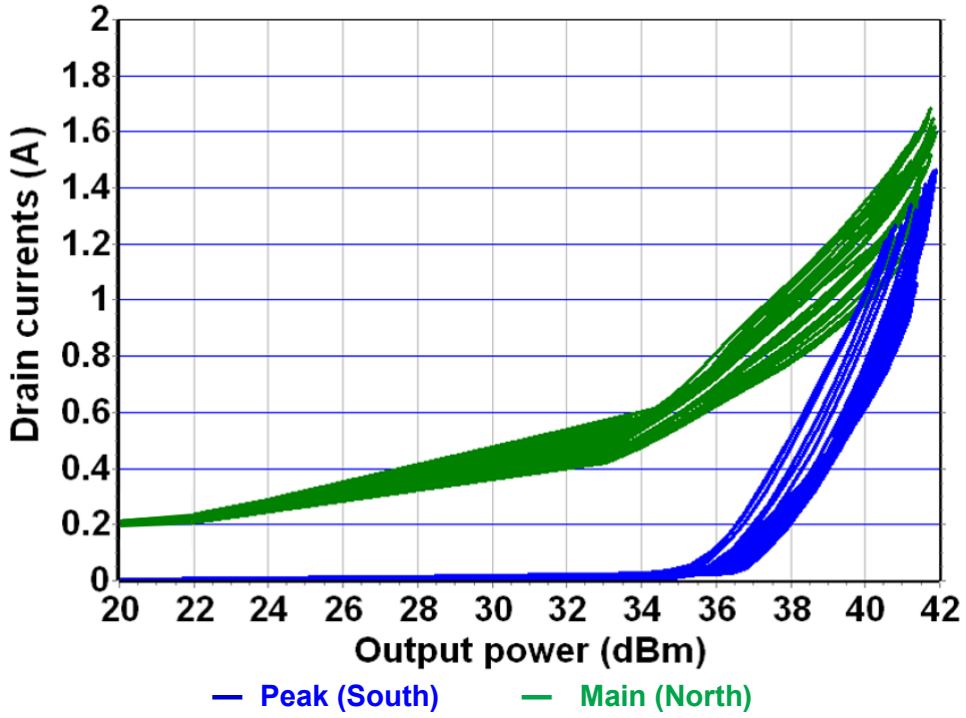
Typical Test Fixture Measurements: Non-linear Performances

CW measurements: $T_{backside}$= 25°C, Vd = +15V, Idq_Main (VGM) = 210mA, Idq_Peak (VGP)=15mA
Pin range : -15 to 20 dBm, Frequency range: 17.2-20.4 GHz step 0.2 GHz

Phase compression vs. Output power



Drain currents vs. Output power



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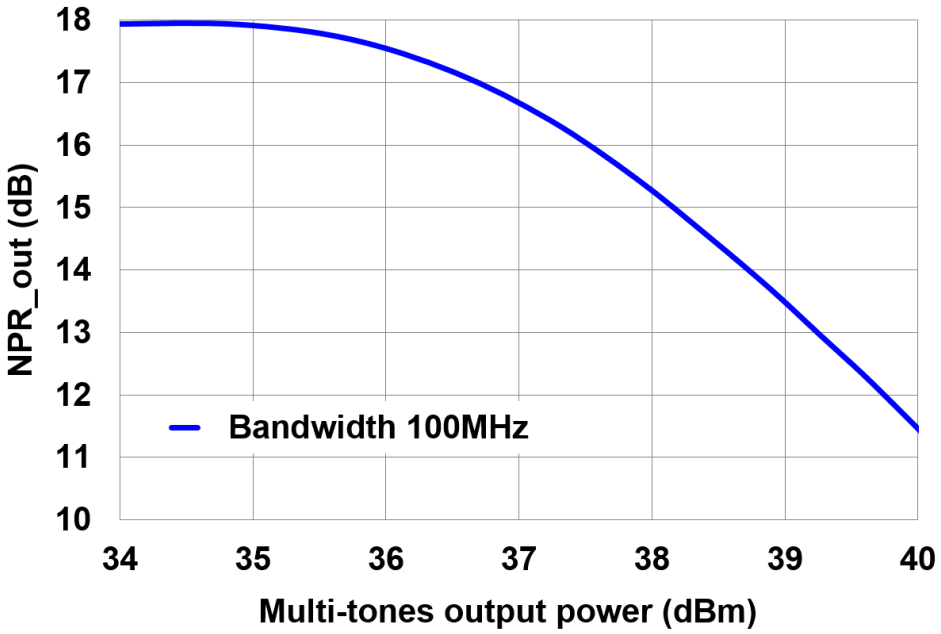
Typical Test Fixture Measurements: NPR Performances

CW measurements: $T_{backside}$= 25°C, Vd = +15V, Idq_Main (VGM) = 210mA, Idq_Peak (VGP)=15mA
Frequency carrier point : 18.75GHz, Instantaneous bandwidth : 100MHz, Noise width : 4%

NPR_out vs. Two-tones output power



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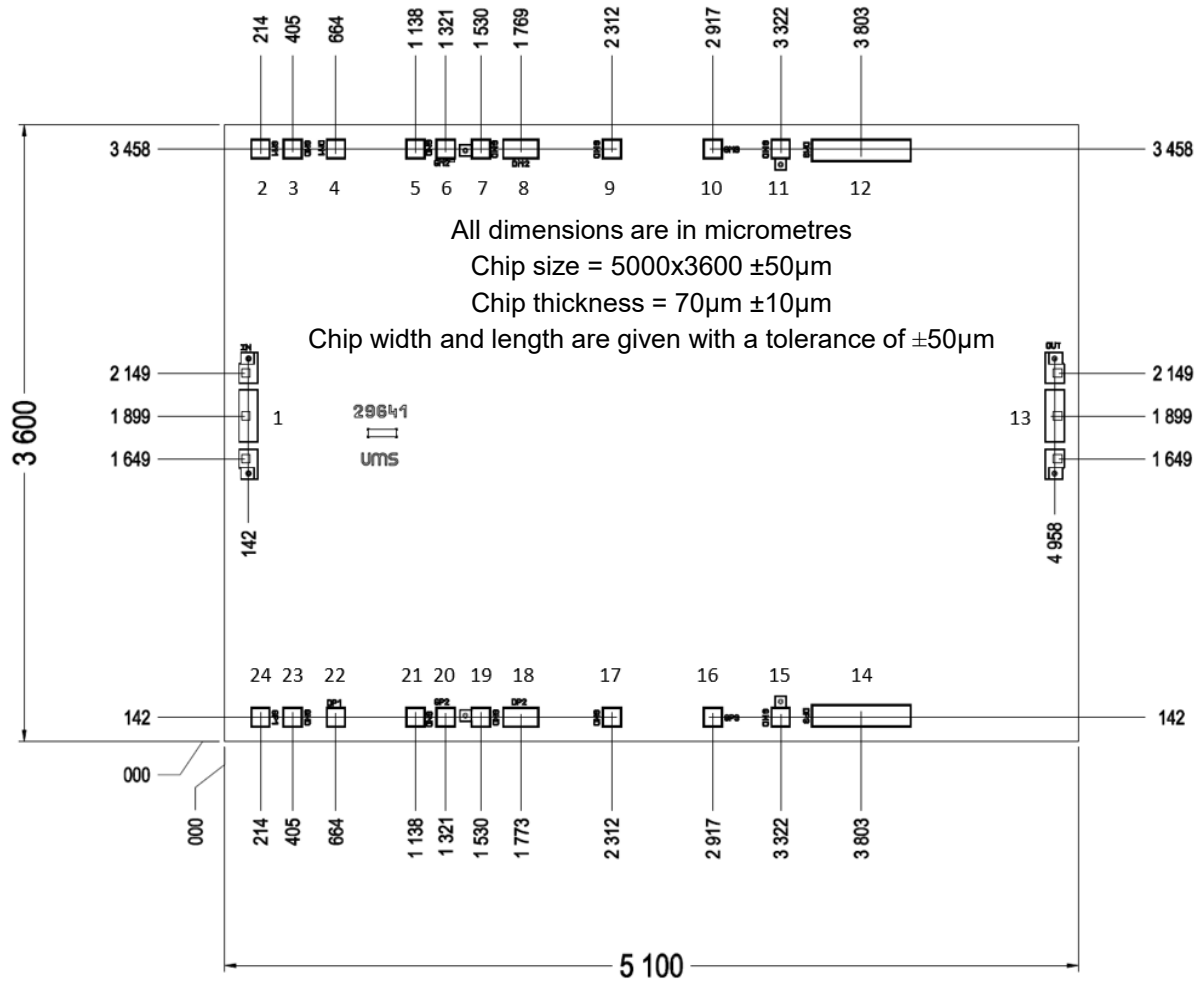
Mechanical Drawing



PAD Number	Name	Description	Pad size
1	IN	RF input	308µm x 118µm
3, 5, 7, 9, 11, 15, 17, 19, 21, 23	GND	Ground (Not connected)	118µm x 118µm
2	GM1	Main gate voltage of 1st	118µm x 118µm
24	GP1	Peak gate voltage of 1st	118µm x 118µm
6	GM2	Main gate voltage of 2nd	118µm x 118µm
20	GP2	Peak gate voltage of 2nd	118µm x 118µm
10	GM3	Main gate voltage of 3rd	118µm x 118µm
16	GP3	Peak gate voltage of 3rd	118µm x 118µm
4	DM1	Main drain voltage of 1st	118µm x 118µm
22	DP1	Peak drain voltage of 1st	118µm x 118µm
8	DM2	Main drain voltage of 2nd	218µm x 118µm
18	DP2	Peak drain voltage of 2nd	218µm x 118µm
12	DM3	Main drain voltage of 3rd	600µm x 134µm
14	DP3	Peak drain voltage of 3rd	600µm x 134µm
13	OUT	RF output	308µm x 118µm

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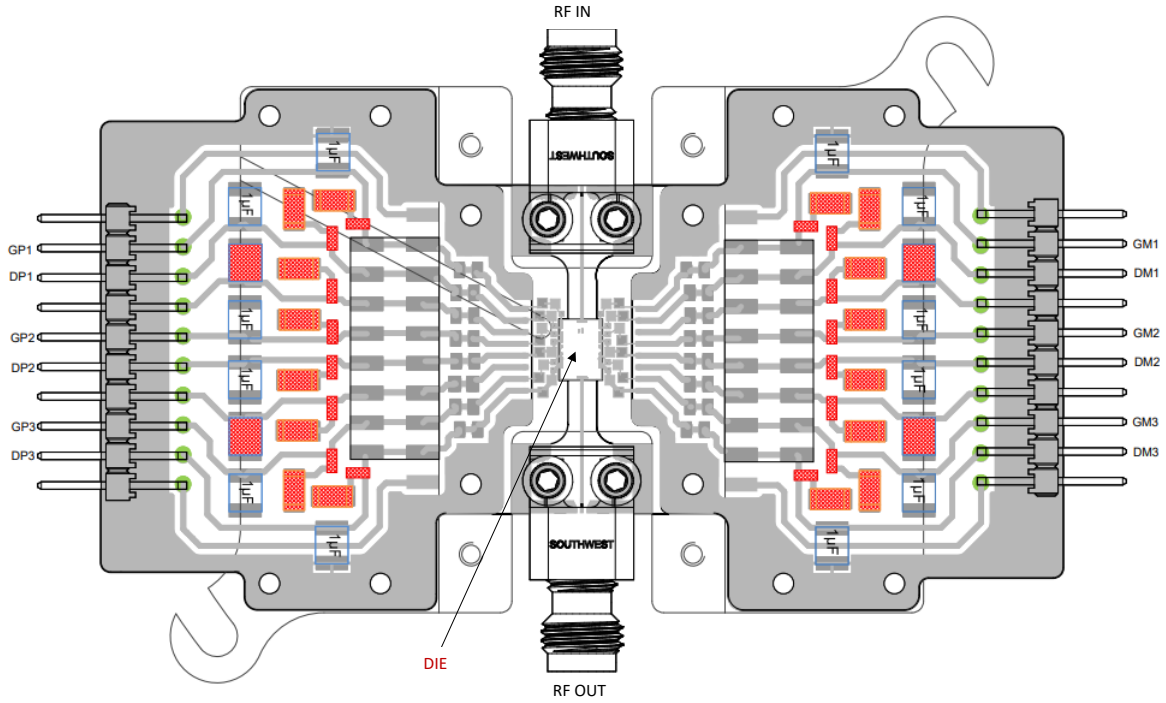
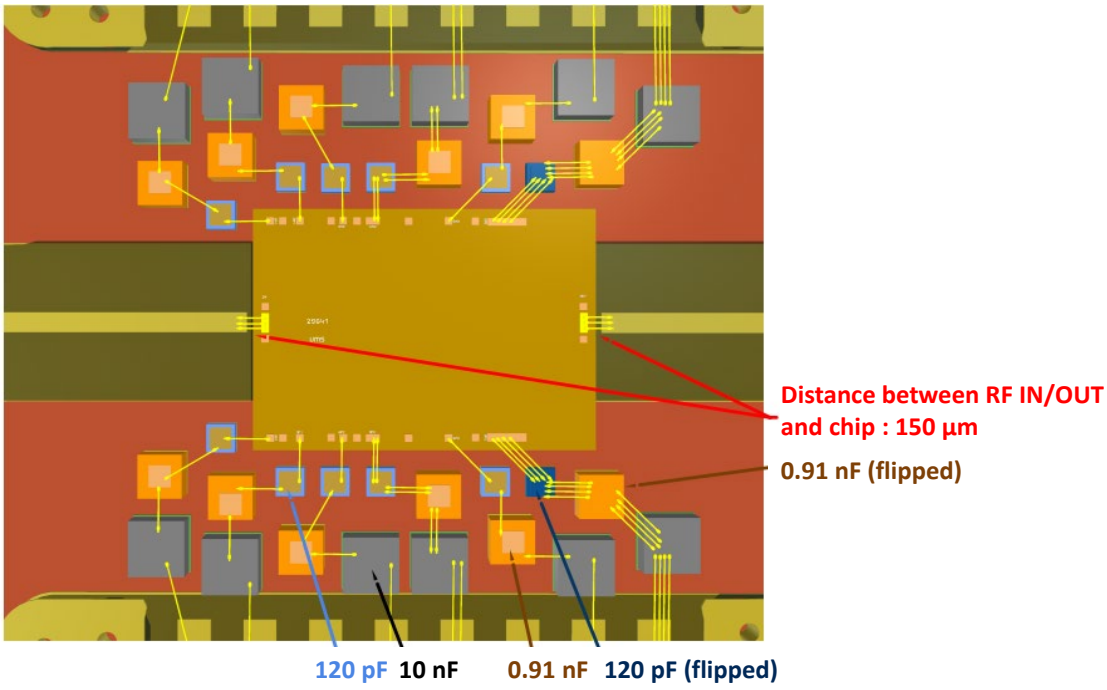
Recommended Assembly Plan





4 levels of decoupling capacitor have been used:
First level of capacitor is 120pF, second level is 0.91nF, third level is 10nF and fourth level is 1µF. Only 120pF, 1nF and 10nF capacitors could be seen on the previous assembly drawing (close to the chip). Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended reflow process assembly

Refer to the application note AN0001 available at https://www.ums-rf.com for die attach.

Recommended Evaluation board assembly

Refer to the application note AN0030 available at https://www.ums-rf.com Evaluation board.

Ordering Information

Chip form:	CHA8254-99F/00

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