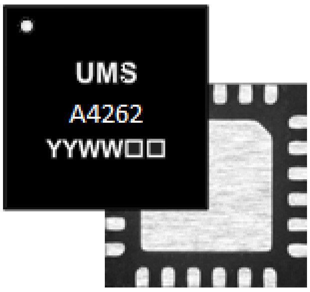
CHA4262-QDG

17 - 22 GHz Medium Power Amplifier

GaAs Monolithic Microwave IC

Description

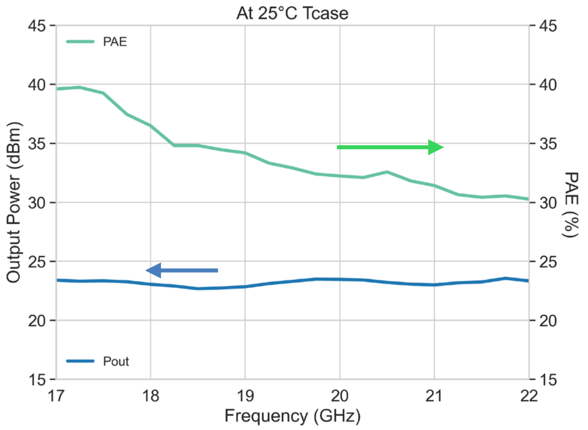
The CHA4262-QDG is a three-stage GaAs Medium Power Amplifier operating between 17GHz and 22GHz. This amplifier provides 23dBm saturated output power with 37% Power Added Efficiency and 20dBm Output Power at 1dB gain compression. The circuit exhibits a typical small signal gain of 26dB and 30dBm Output Third-Order Intercept Point.
This Medium Power Amplifier is dedicated to Space applications and it is also ideal for a wide range of microwave systems.
This new product is matched to 50Ω and supplied on RoHS 4 mm x 4 mm QFN plastic package.



Main Features

- ■ Frequency band: 17-22GHz
- ■ 23dBm P_{OUT} at 37% PAE
- ■ 26dB small signal gain
- ■ NPR = 12dBc at 22dBm Average Pout[(1)]
- ■ Typical DC bias: V_D = 2.5V@I_{DQ} = 130mA
- ■ 24L-QFN 4x4mm^2
- ■ MSL3

(1) *Bandwidth = 1GHz, Notch = 10%*



Main Electrical Characteristics

T_{case}= +25°C, Vd = +2.5V (T_{case} : QFN backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Frequency	Frequency range	17		22	GHz
Gain	Small signal Gain		26		dB
P_{SAT}	Saturated Output power (Pin = 5dBm)		23		dBm
PAE	Power Added Efficiency (Pin = 5dBm)		37		%
NPR	Noise power ratio (Pin = 5dBm)		12		dBc
I_{DQ}	Quiescent Drain Current		130		mA

Electrical Characteristics

T_{case}= +25°C, Vd = +2.5V (T_{case} : QFN backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17		22	GHz
Gain	Small Signal Gain		26		dB
IRL	Input return loss		-13		dB
ORL	Output return loss		-13		dB
Psat	Saturated Output power (Pin = 5dBm)		23		dBm
P1dB	Output Power @1dB Gain compression		20		dBm
OIP3	Output Third-Order Intercept Point		30		dBm
NPR	Noise power ratio (Pin = 5dBm)		12		dB
PAE	Power Added Efficiency (Pin = 5dBm)		37		%
NF	Noise Figure		3.5		dB
I_{DQ}	Quiescent Drain Current		130		mA

These values are representative of on-board measurements as defined on the drawing in paragraph "Evaluation board".

Absolute Maximum Ratings (1)

T_{case}= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	3.5V	V
Id	Drain bias current	200	mA
Vg	Gate bias voltage	-2 to +0.4	V
Pin	Maximum peak input power overdrive	+7	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range (2), (3)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	2 to 3	V
I_{DQ}	Quiescent Drain Current	90 to 150	mA
Vg	Gate voltage (typical)	-0.45	V
Pin	Maximum peak input power overdrive (2)	+5	dBm
Tj	Junction temperature	175	°C
T_{case}	QFN backside temperature range	-30 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

(2) Electrical performances are defined for specified test conditions

(3) Electrical performances are not guaranteed over all recommended operating conditions

Typical Bias Conditions

T_{case} = +25°C

Symbol	Parameter	Value	Unit
VG1, VG2, VG3	Typical gate bias voltage tuned for I_{DQ} = 130mA	-0.45	V
VD1, VD2, VD3	Drain bias voltage	2.5	V

"Power ON" sequence

1. Ground the device
2. Set the gate voltage to -1.5V
3. Apply the drain voltage Vd (typically +2.5V)
4. Increase Vg up to quiescent bias drain current I_{DQ}
5. Apply RF signal

"Power OFF" sequence

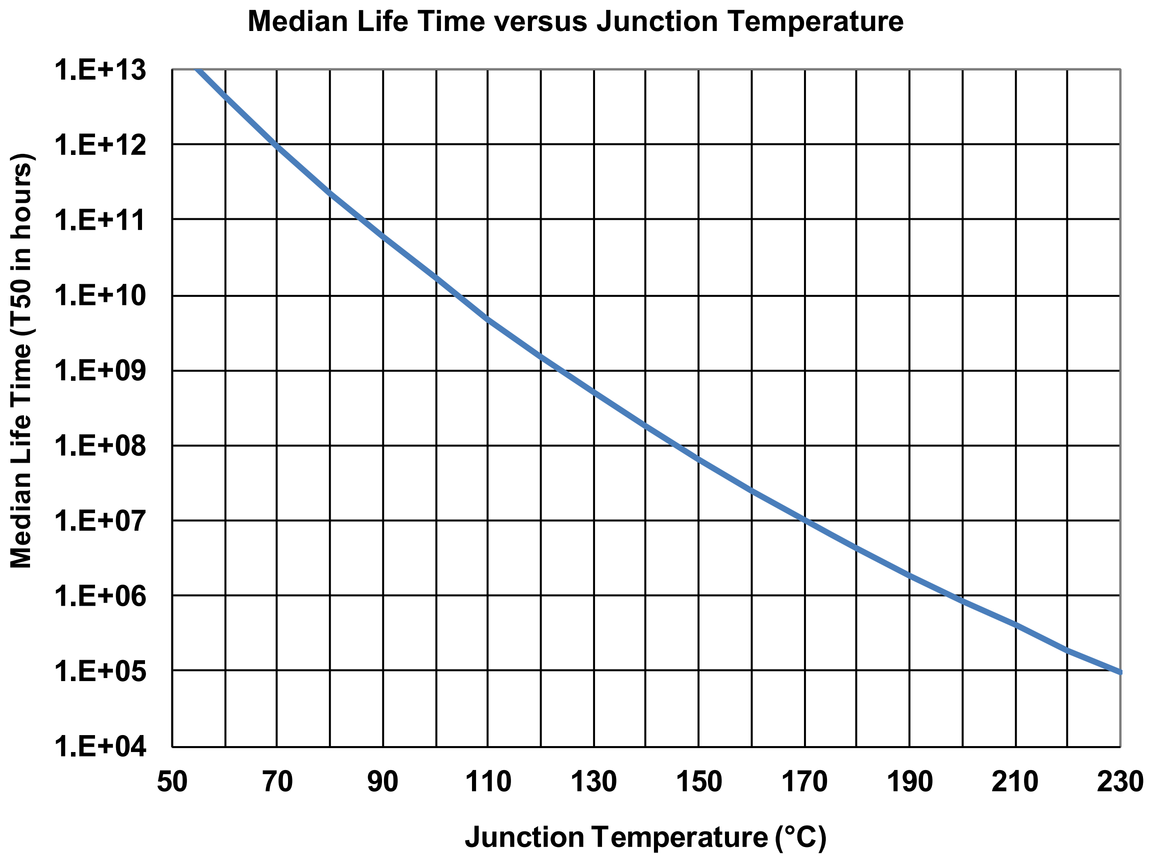
1. Turn off RF signal
2. Decrease the gate voltage to -1.5V
3. Decrease the drain voltage to 0V
4. Turn off Vd supply
5. Turn off Vg supply

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package backside interface (T_{case}).
For nominal operating conditions, the system maximum temperature must be adjusted in order to guarantee that Tj remains below the maximum value specified in the Recommended Operating Ratings table. The system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	T_J (°C)	RTH (°C/W)	T50 (hours)
RTH (1) Thermal Resistance (Junction to QFN Backside)	Vd=2.5V Pout=23dBm Pdiss=0.45W	102	37.2	1.27E+10
	Vd=2.5V Small Signal Pdiss=0.3W	98	40.7	2.09E+10

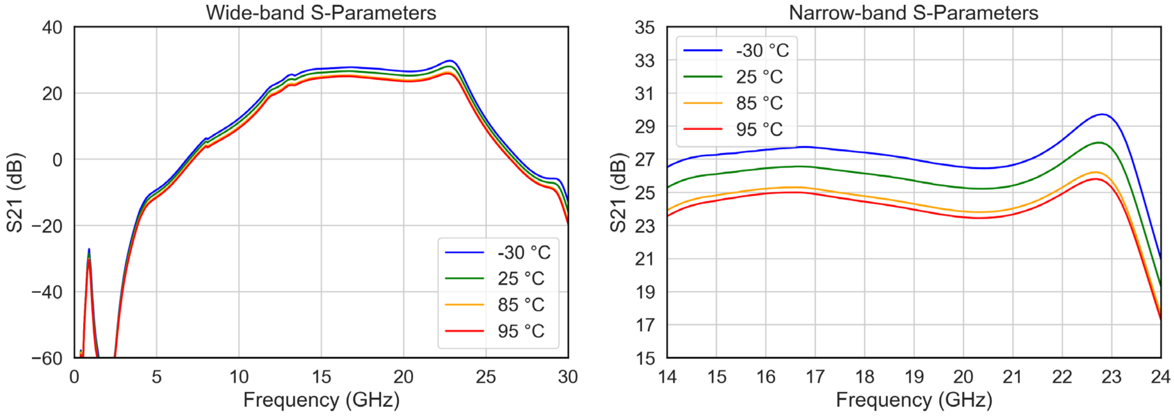
(1) Assuming 85°C T_{case}



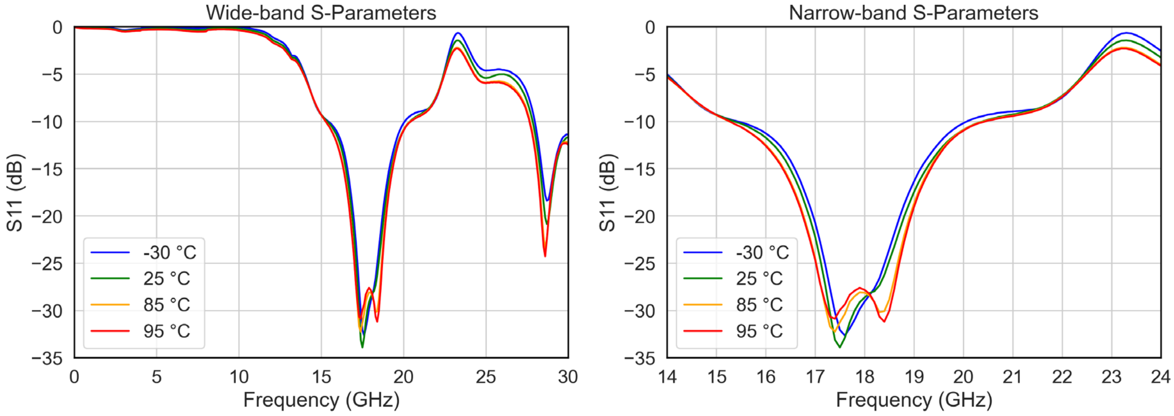
Typical on Board Measurements

Test conditions : T_{case}= -30°C/+25°C/85°C/95°C, Vd = 2.5V, Idq = 130mA
Board losses are de-embedded. Measurements are given in the package access plans.

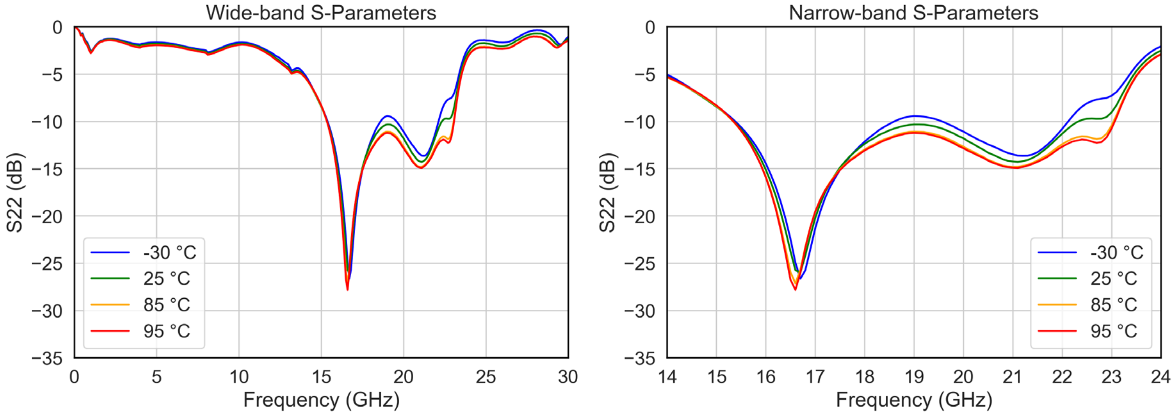
Linear Gain vs. Frequency & Temperature



Input Return Loss vs. Frequency & Temperature



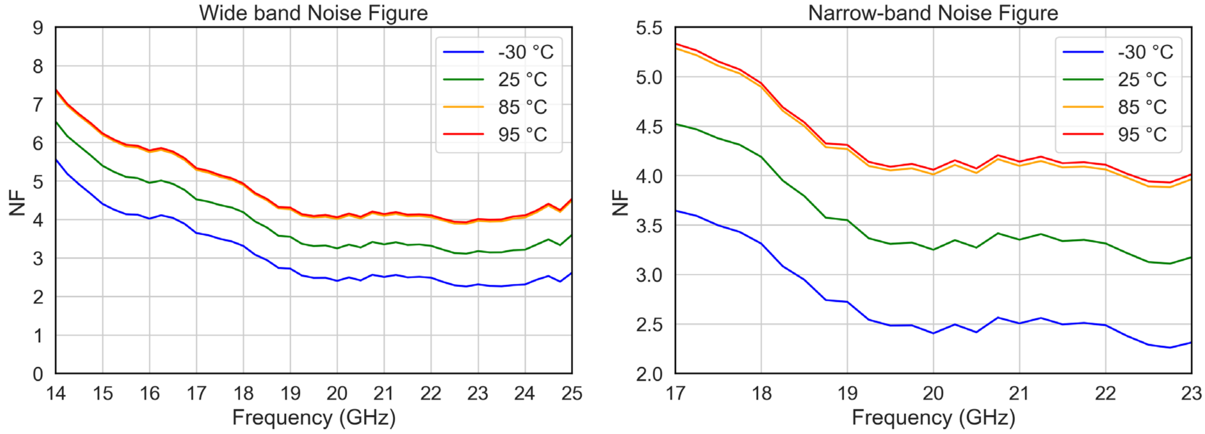
Output Return Loss vs. Frequency & Temperature



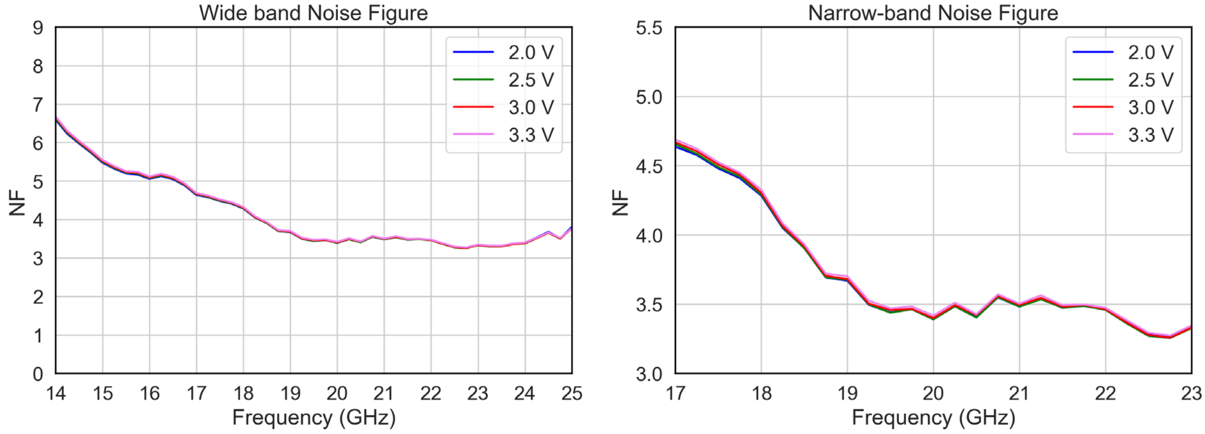
Typical Board Measurements

Test conditions : T_{case} = -30°C/+25°C/85°C/95°C, Vd = 2V/2.5V/3V/3.3V,
Idq = 90mA/130mA/150mA
Board losses are de-embedded. Measurements are given in the package access plans.

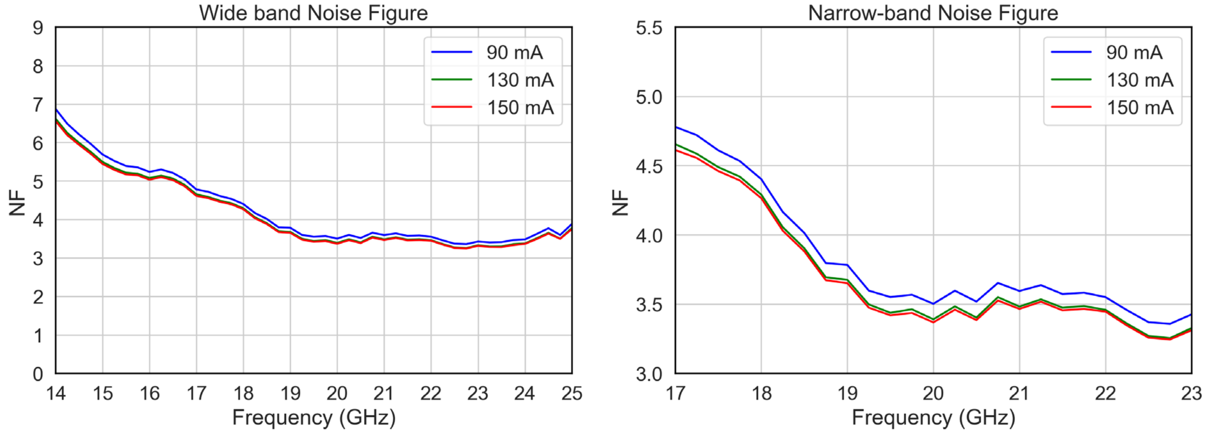
Noise Figure vs. Frequency & Temperature at Vd = 2.5V & Idq = 130mA



Noise Figure vs. Frequency & Drain voltage at Idq = 130mA & Temp = 25°C



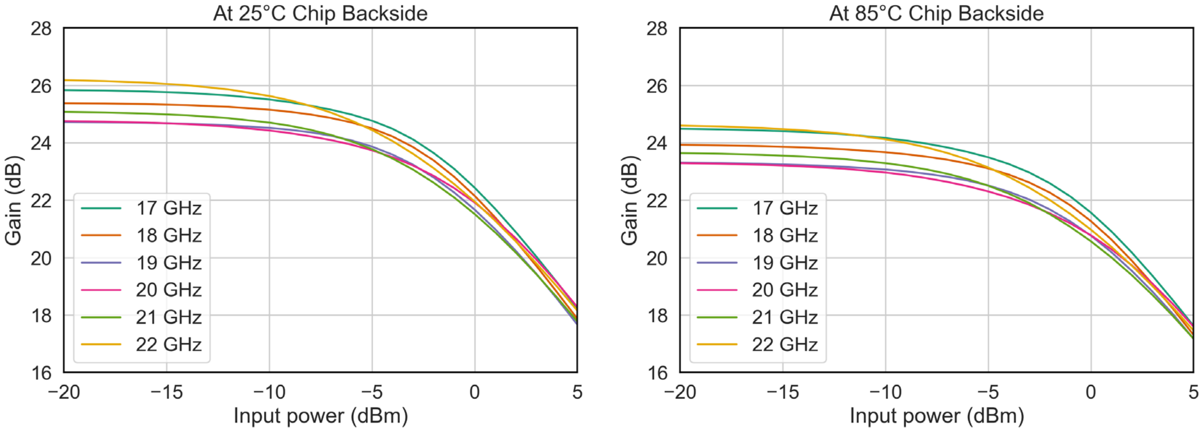
Noise Figure vs. Frequency & Current at Vd = 2.5V & Temp = 25°C



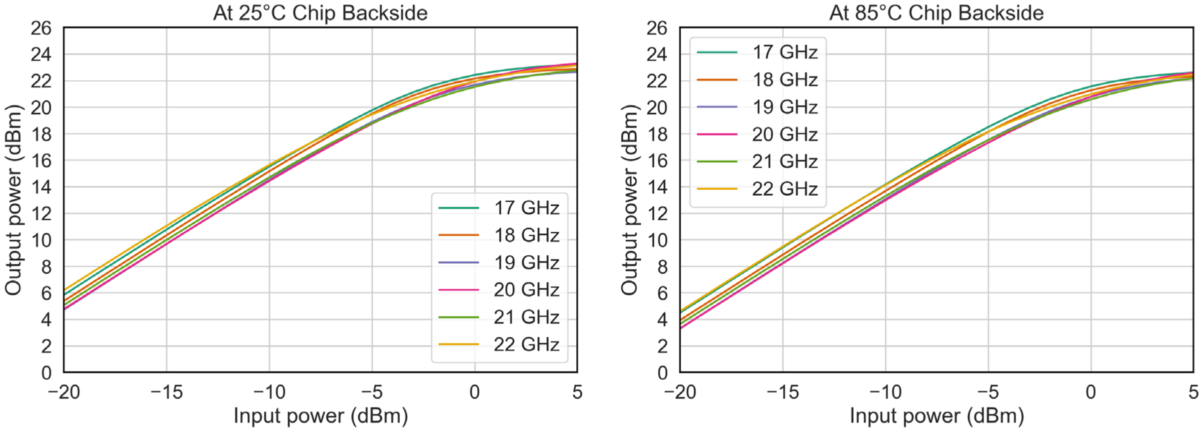
Typical Board Measurements

Test conditions : T_{case} = +25°C/85°C, Vd = 2.5V, Idq = 130mA
Board losses are de-embedded. Measurements are given in the package access plans.

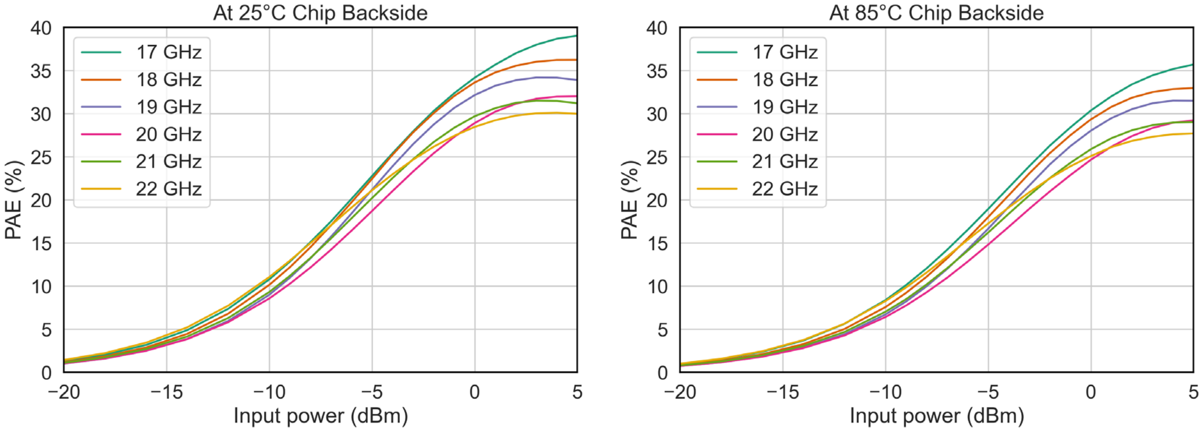
Gain vs. Input Power & Frequency



Output Power vs. Input Power & Frequency



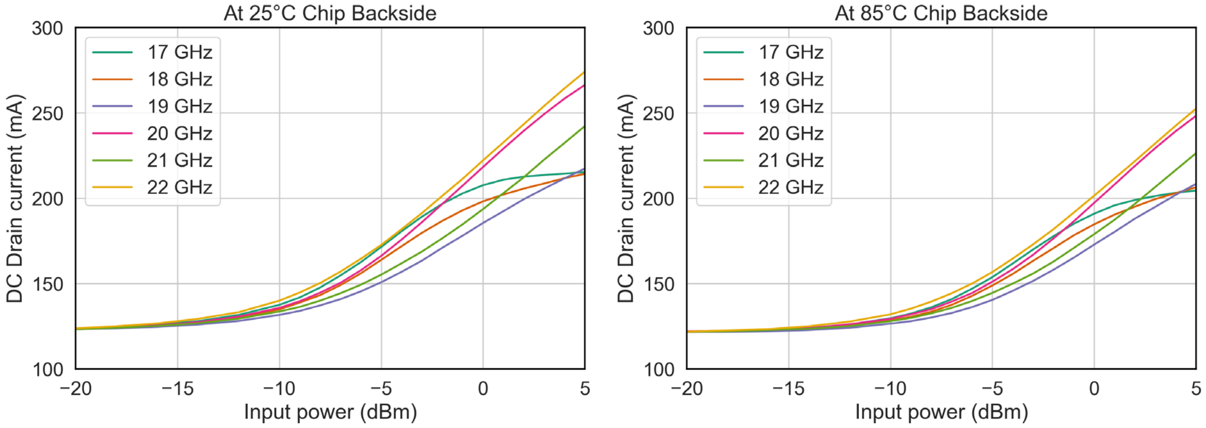
Power Added Efficiency vs. Input Power & Frequency



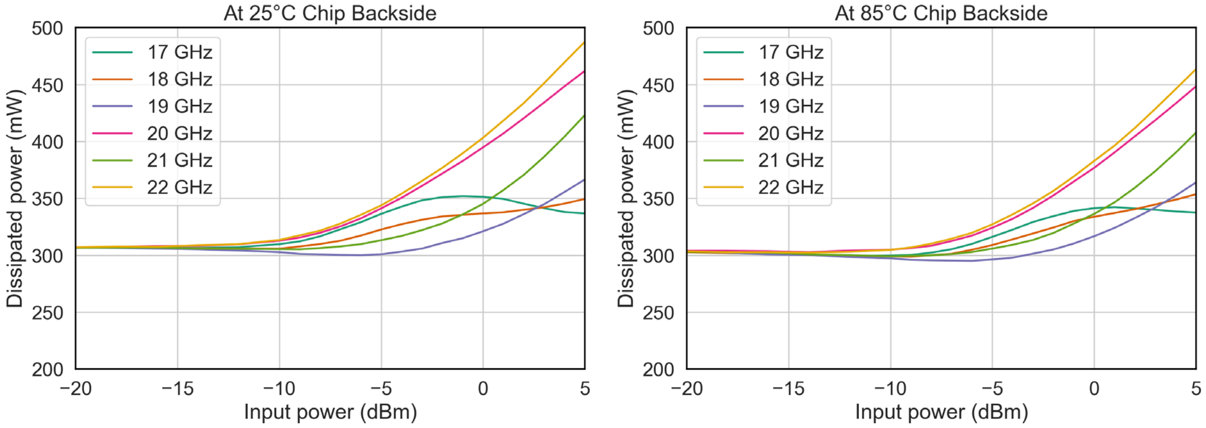
Typical Board Measurements

Test conditions : T_{case} = +25°C/85°C, Vd = 2.5V, Idq = 130mA
Board losses are de-embedded. Measurements are given in the package access plans.

Drain Current vs. Input Power & Frequency



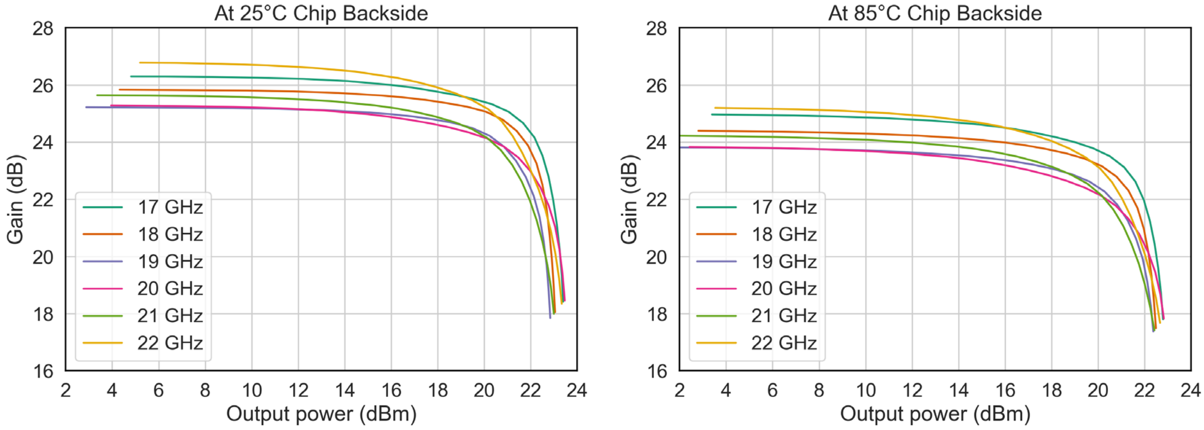
Dissipated Power vs. Input Power & Frequency



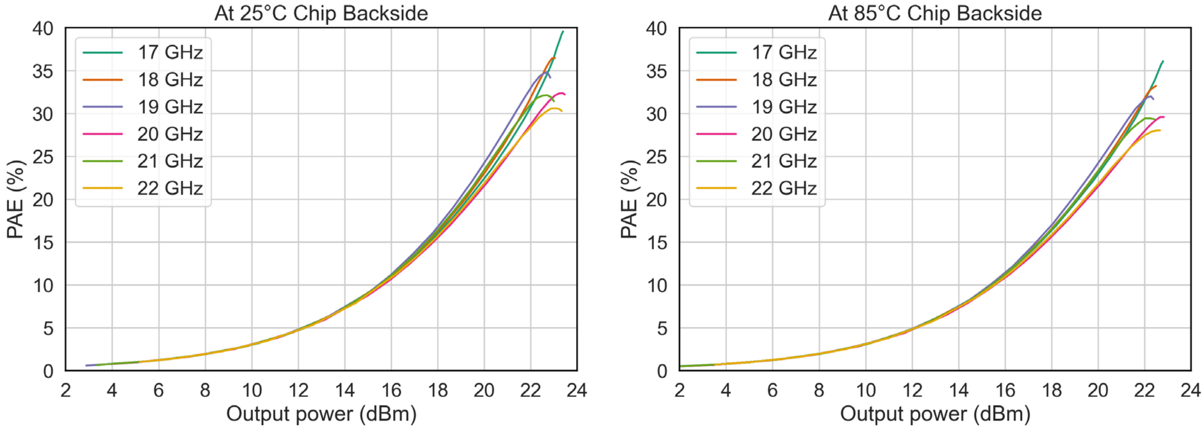
Typical Board Measurements

Test conditions : T_{case} = +25°C/85°C, Vd = 2.5V, Idq = 130mA
Board losses are de-embedded. Measurements are given in the package access plans.

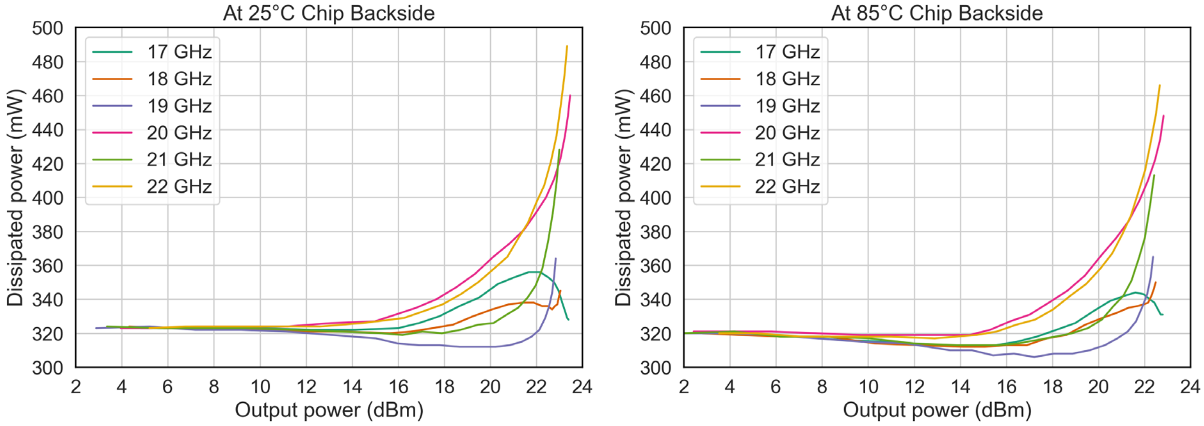
Gain vs. Output Power & Frequency



Power Added Efficiency vs. Output Power & Frequency



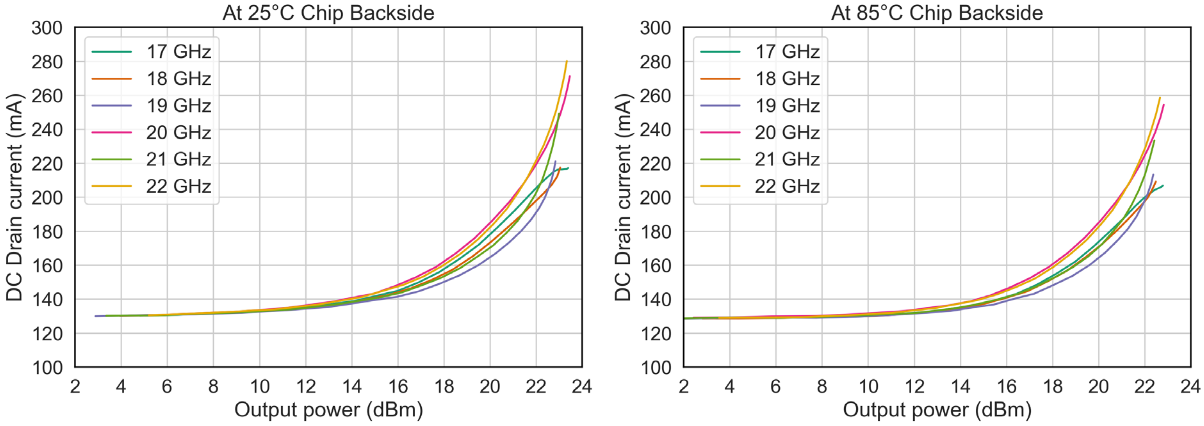
Dissipated Power vs. Output Power & Frequency



Typical Board Measurements

Test conditions : T$_{case}$ = +25°C/85°C, Vd = 2.5V, Idq = 130mA
Board losses are de-embedded. Measurements are given in the package access plans.

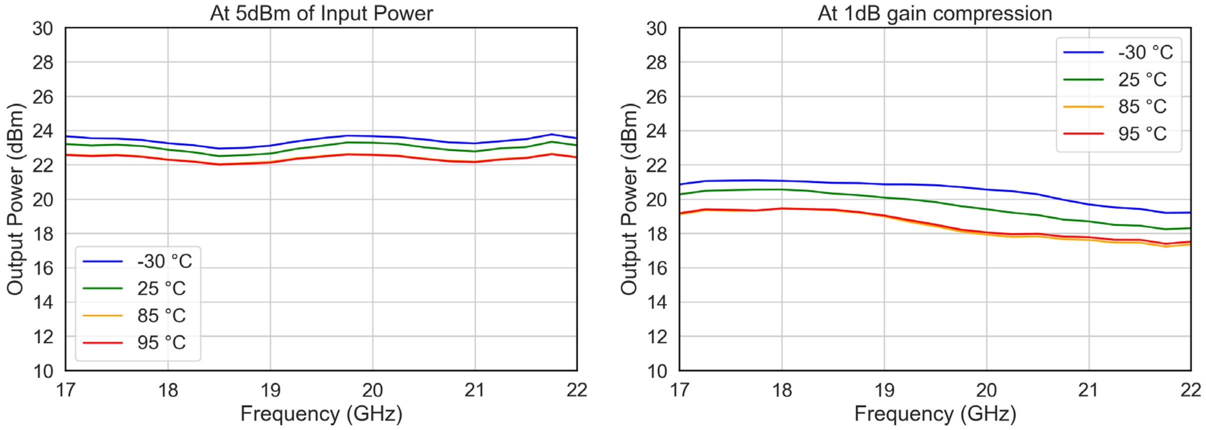
Drain Current vs. Output Power & Frequency



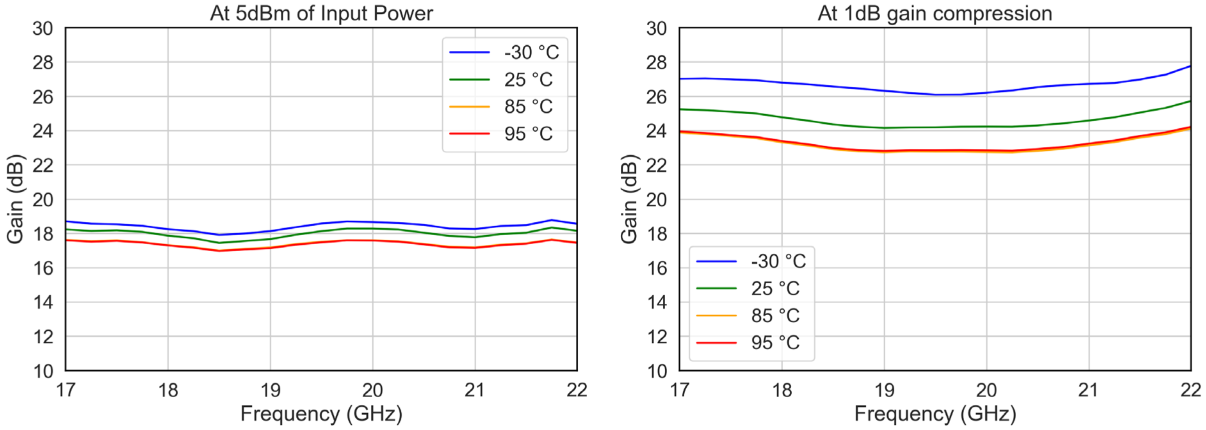
Typical Board Measurements

Test conditions : T$_{case}$ = -30°C/+25°C/85°C/95°C, Vd = 2.5V, Idq = 130mA
Board losses are de-embedded. Measurements are given in the package access plans.

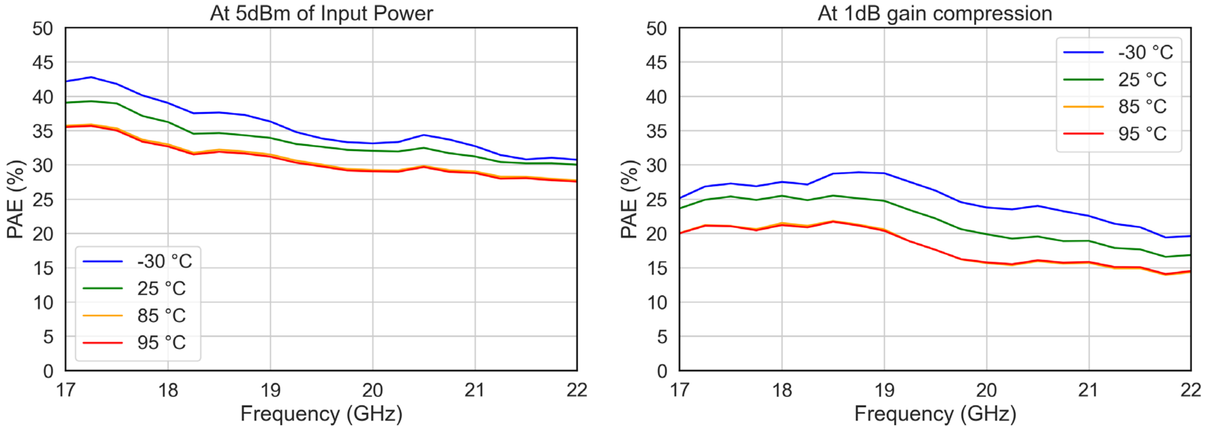
Output Power vs. Frequency & Temperature



Gain vs. Frequency & Temperature



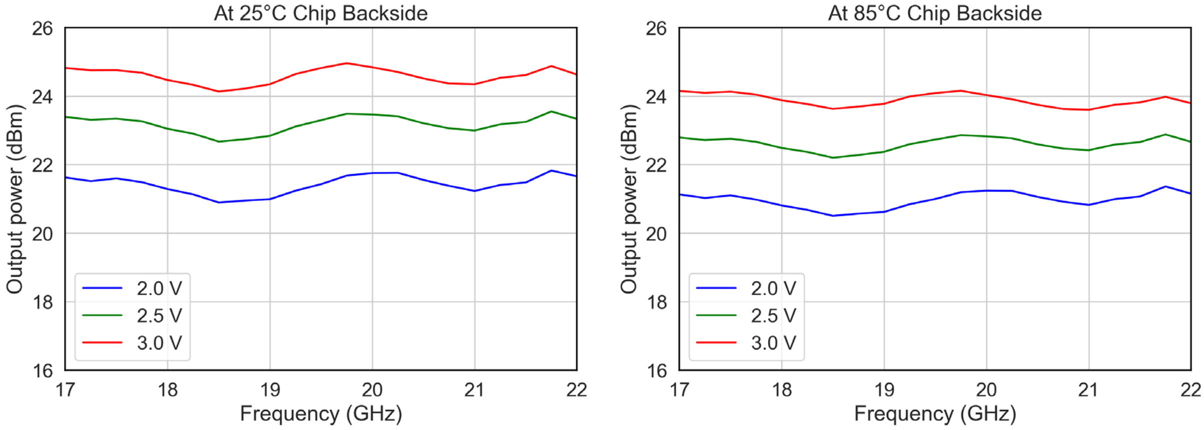
Power Added Efficiency vs. Frequency & Temperature



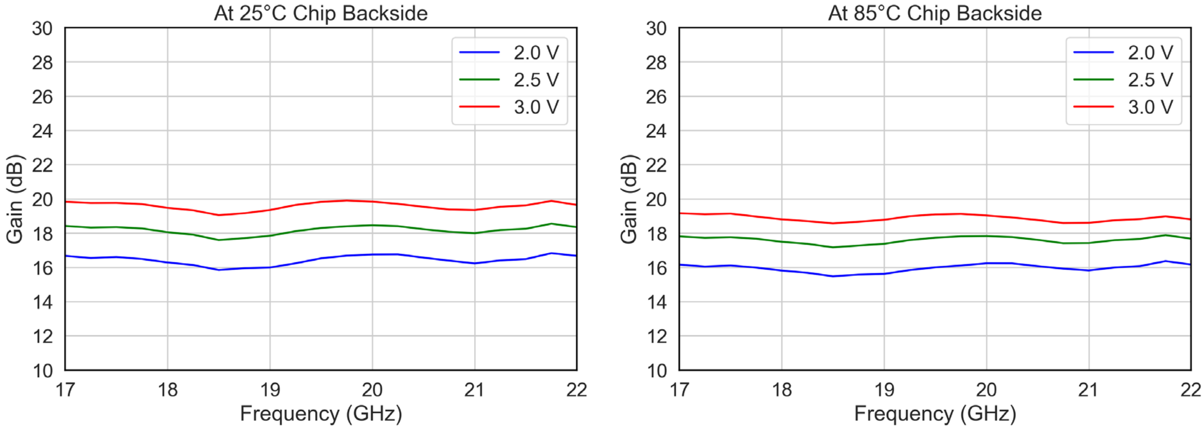
Typical Board Measurements

Test conditions : T_{case} = 25°C, Vd = 2V/2.5V/3V, Idq = 130mA, Pin=5dBm
Board losses are de-embedded. Measurements are given in the package access plans.

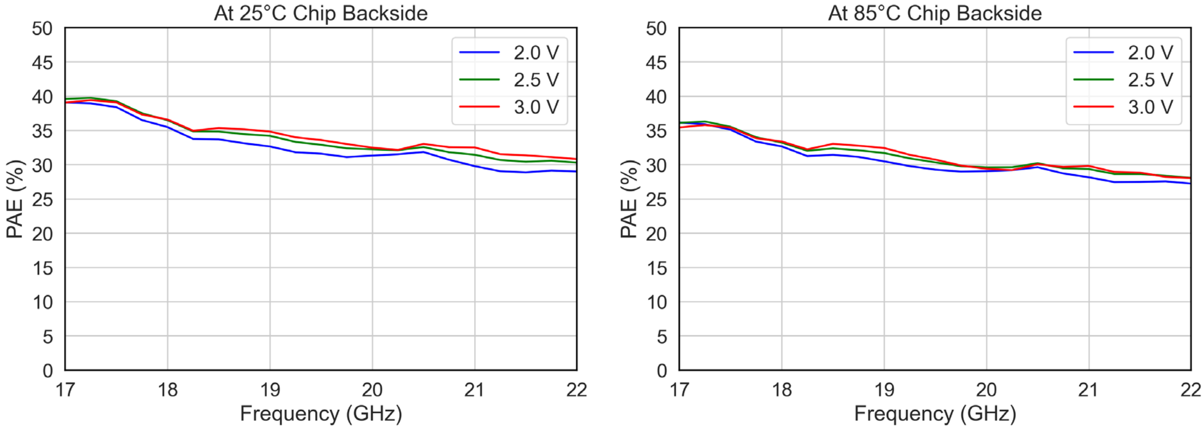
Output Power vs. Frequency & Vd



Gain vs. Frequency & Vd



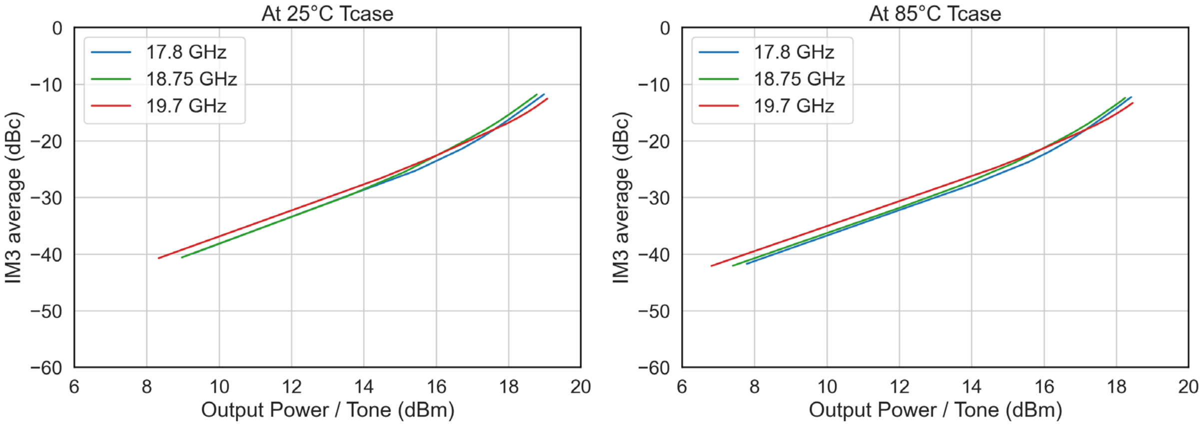
Power Added Efficiency vs. Frequency & Vd



Typical Board Measurements

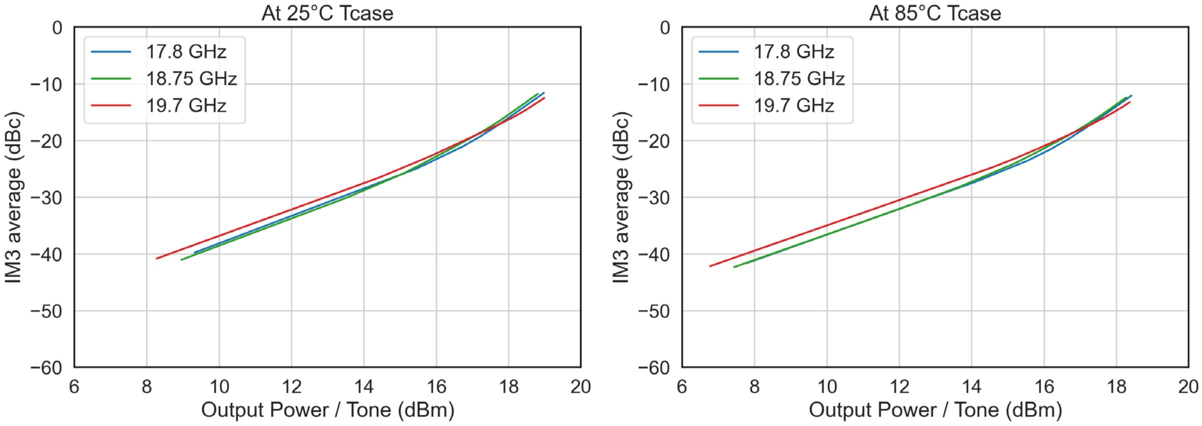
Test conditions : CW dual tones, Vd = +2.5V, Idq = 130mA, Δf = 10MHz, T_{case} = +25°C/85°C

IMD3 vs. Output Power per Tone & Frequency



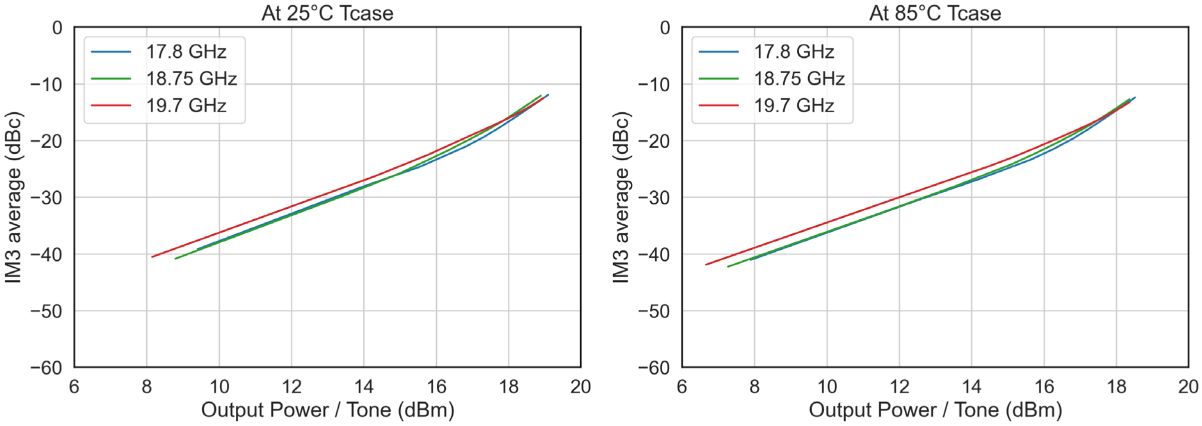
Test conditions : CW dual tones, Vd = +2.5V, Idq = 130mA, Δf = 50MHz, T_{case} = +25°C/85°C

IMD3 vs. Output Power per Tone & Frequency



Test conditions : CW dual tones, Vd = +2.5V, Idq = 130mA, Δf = 100MHz, T_{case} = +25°C/85°C

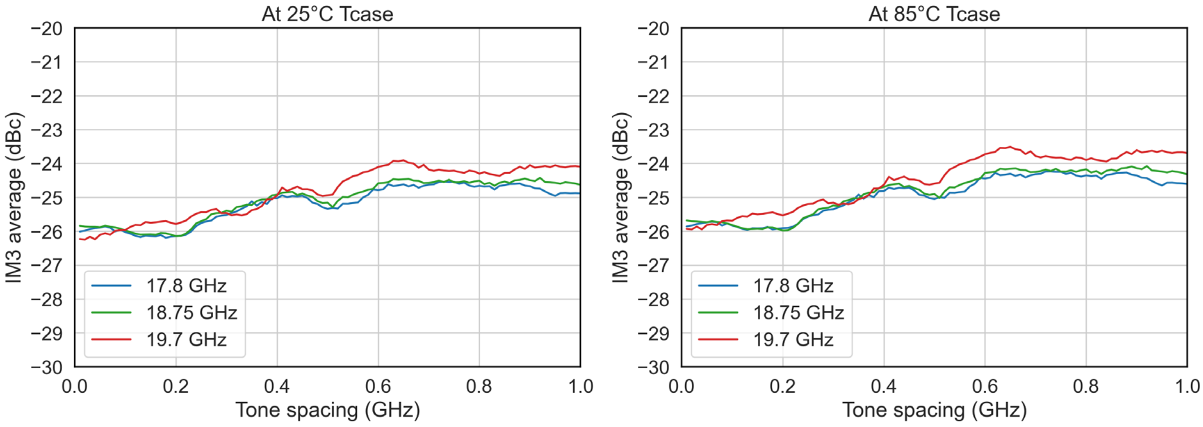
IMD3 vs. Output Power per Tone & Frequency



Typical Board Measurements

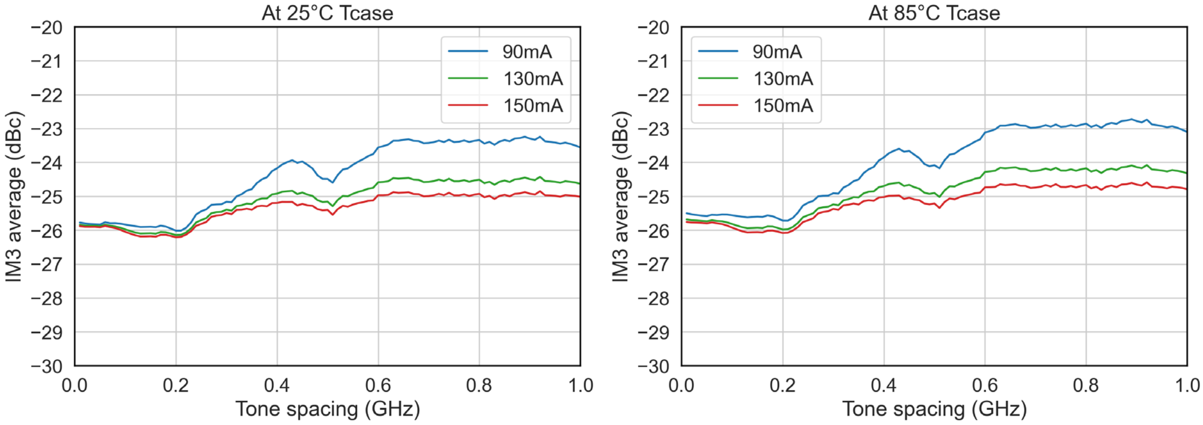
Test conditions : CW dual tones, Vd = +2.5V, Idq = 130mA, Pout/tone = 14dBm, T_{case} = +25°C/85°C

IMD3 vs. Tone Spacing & Frequency



Test conditions : CW dual tones, Vd = +2.5V, Fc = 18.75GHz, Pout/tone = 14dBm, T_{case} = +25°C/85°C

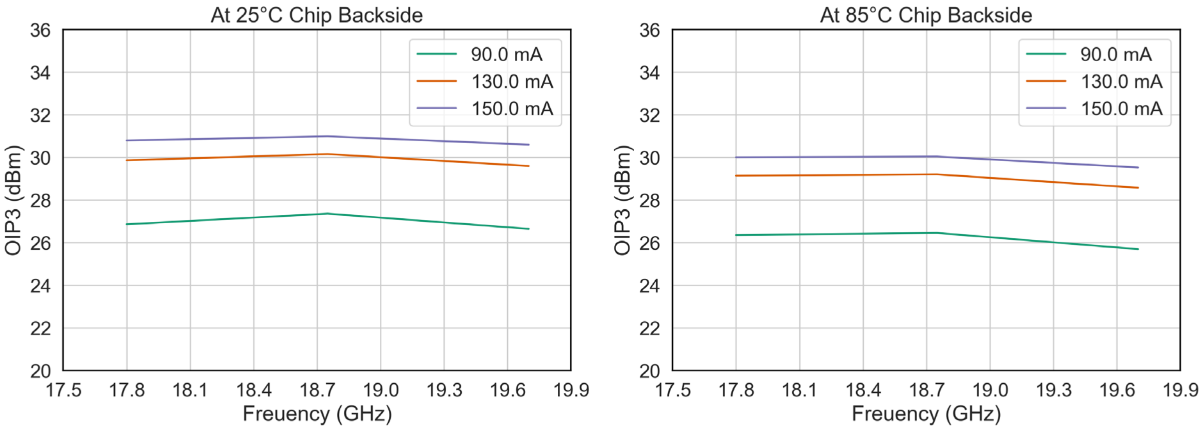
IMD3 vs. Tone Spacing & Drain Current



Typical Board Measurements

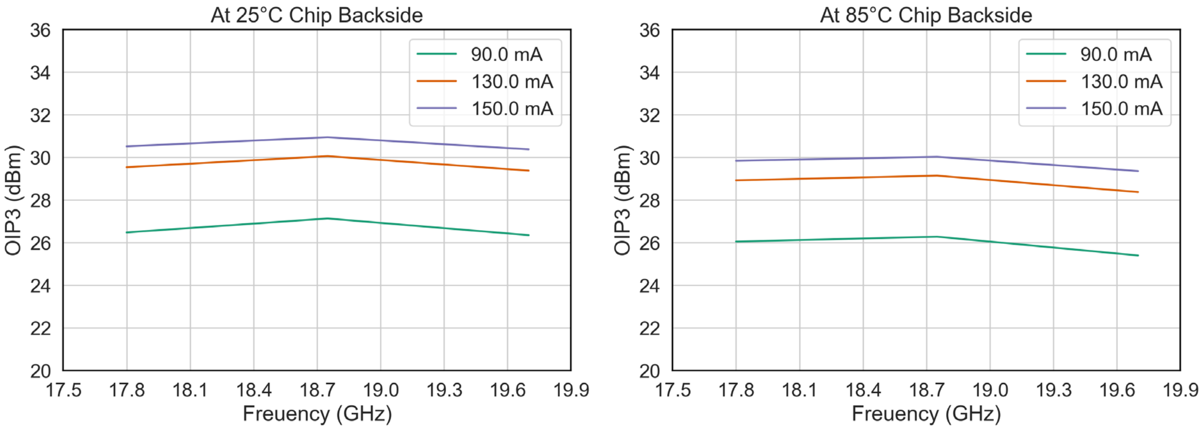
Test conditions : CW dual tones, Vd = +2.5V, Idq = 90,130,150mA, ∆f = 10MHz, Pout/tone = -15dBm,

OIP3 vs. Frequency & Quiescent Drain Current



Test conditions : CW dual tones, Vd = +2.5V, Idq = 90,130,150mA, ∆f = 100MHz, Pout/tone = -15dBm

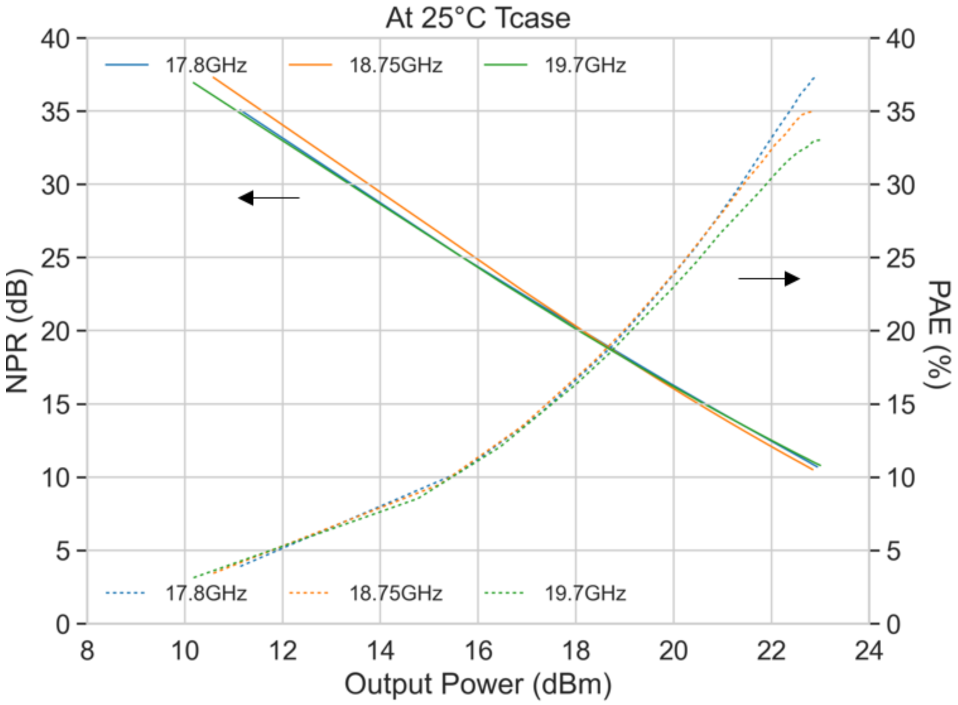
OIP3 vs. Frequency & Quiescent Drain Current



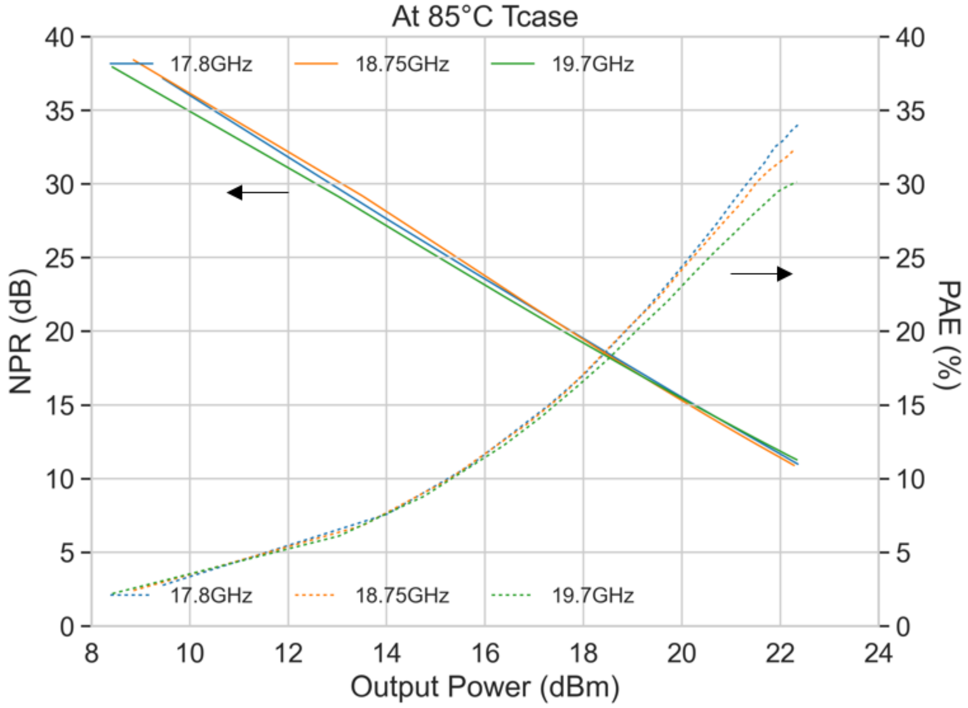
Typical Board Measurements

Test conditions : Vd = +2.5V, Idq = 130mA, T_{case} = +25°C/85°C, Bandwidth = 1GHz, Notch = 10%

NPR and PAE vs. Output Power & Frequency

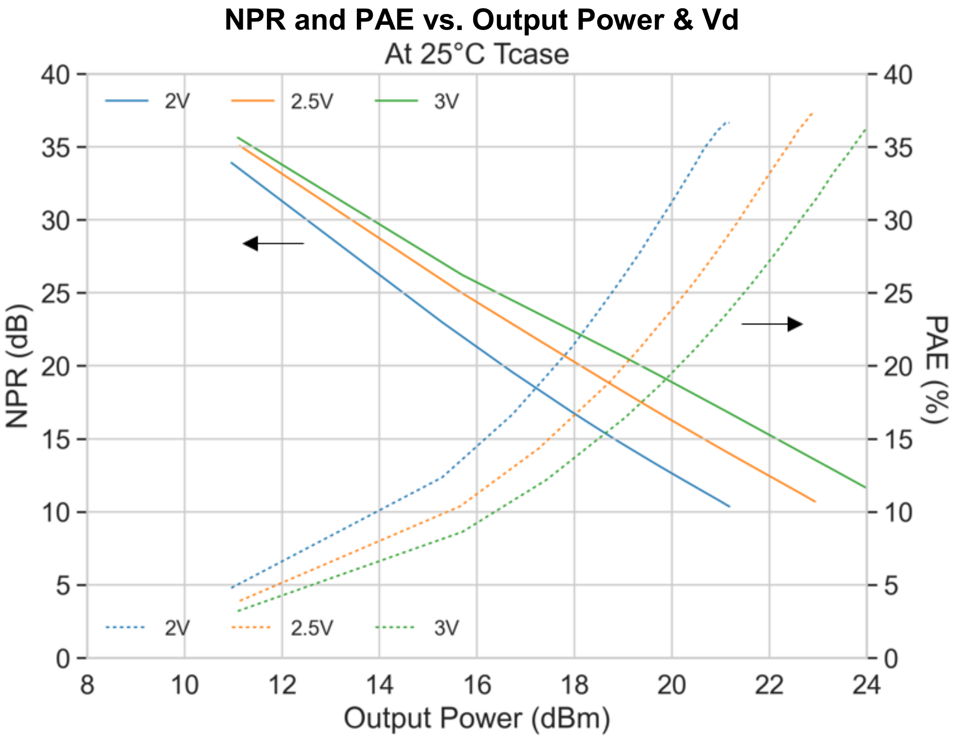


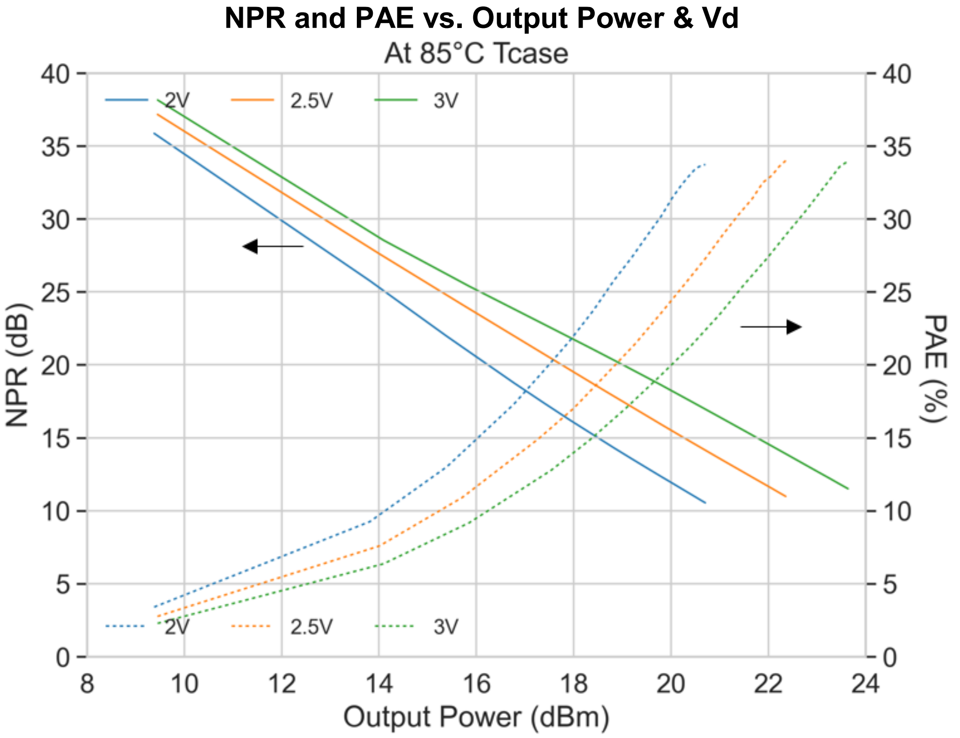
NPR and PAE vs. Output Power & Frequency



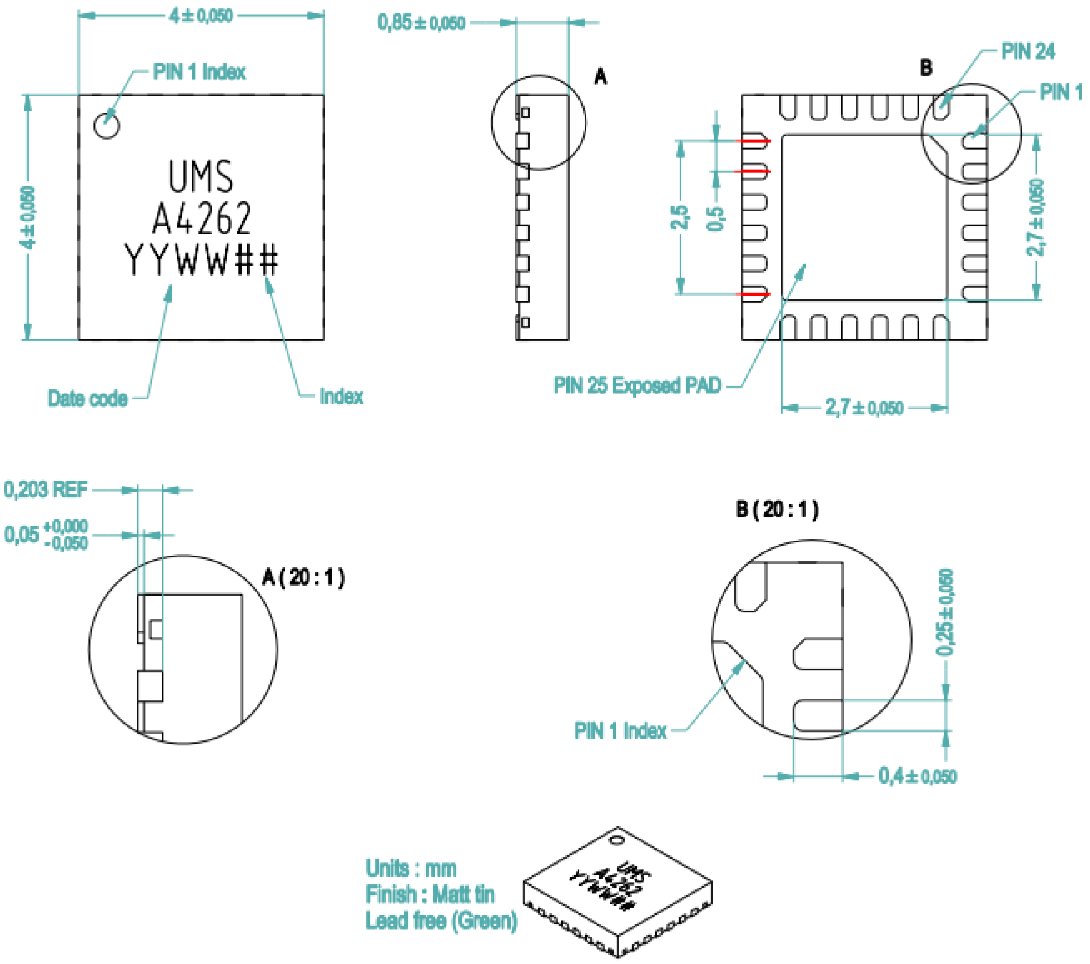
Typical Board Measurements

Test conditions : Vd = +2V/+2.5V/+3V, Idq = 130mA, T_{case} = +25°C/85°C , Bandwidth = 1GHz, Notch = 10%, Freq = 17.8GHz





Package outline (1)

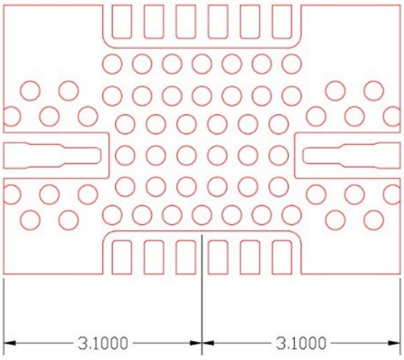


Finish:	Matt tin Lead Free (Green)	1- NC	10- VG3	19- NC
Units :	mm	2- GND(1)	11- GND(1)	20- GND(1)
From the standard :	JEDEC MO-220	3- GND(1)	12- NC	21- VD3
	(VGGD)	4- RF IN	13- GND(1)	22- VD2
NC :	Not Connected	5- GND(1)	14- GND(1)	23- VD1
		6- GND(1)	15- RF OUT	24- NC
		7- NC	16- GND(1)	25- GND(1)
		8- VG1	17- GND(1)	
		9- VG2	18- NC	

(1) It is strongly recommended to ground all pins marked “GND” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Definition of measurement reference planes

The reference planes used for measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.1mm offset (input wise and output wise respectively) from this axis.



ESD sensitivity

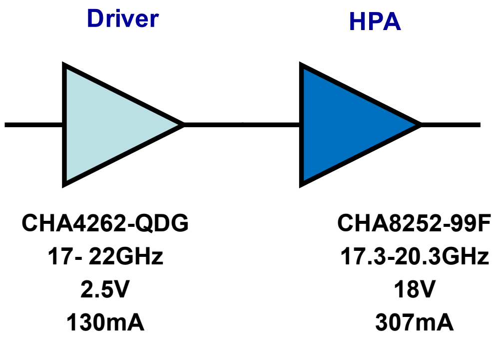
Parameter	Classification	Standard
Human Body Model (HBM)	1A	ANSI/ESDA/JEDEC - JS-001

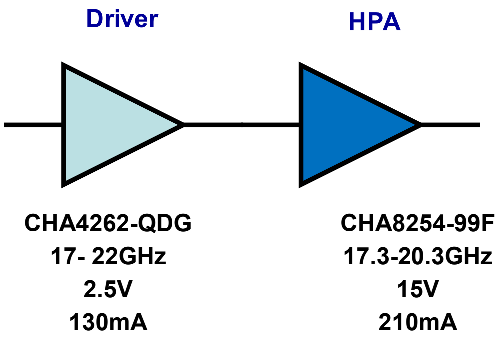
Package Information

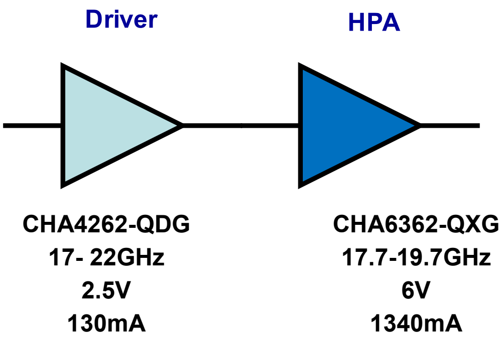
Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% Matt Tin
Moisture Sensitivity Level	MSL3

Recommended UMS Power chain

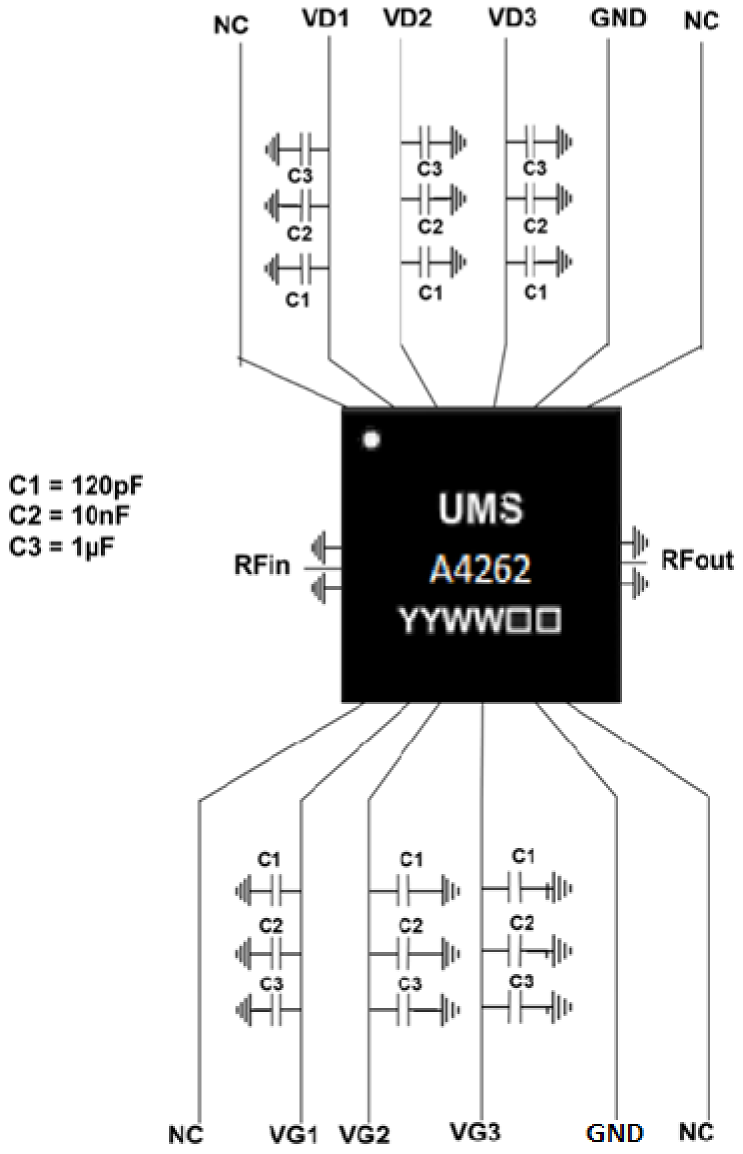
The CHA4262-QDG is recommended with different HPA.
For more information about the CHA8252-99F, the CHA8254-99F and the CHA6362-QXG see our web site https://www.ums-rf.com







Recommended assembly plan



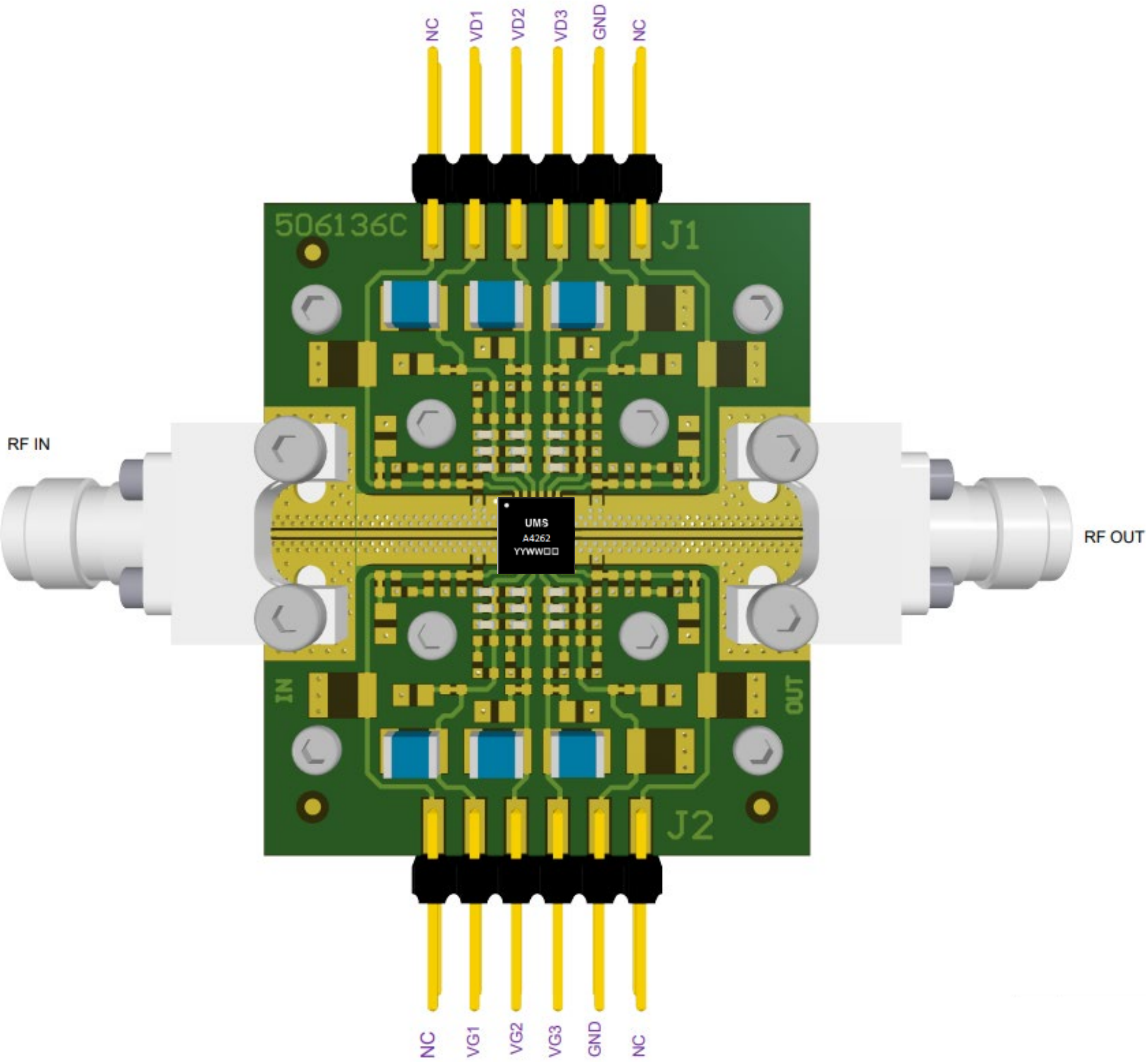
Recommended circuit bonding table

Label	Pin	Type	Decoupling	Comment
RF IN, RF OUT	4, 15	RF access	NA	-
VD1, VD2, VD3	23, 22, 21	Vd	120pF, 10nF & 1µF	Drain Supply
VG1, VG2, VG3	8, 9, 10	Vg	120pF, 10nF & 1µF	Gate Supply

Evaluation board

- ■ Compatible with the proposed footprint.
- ■ Based on typically Ro4350B / 8mils or equivalent.
- ■ Using a micro-strip to coplanar transition to access the package.
- ■ Recommended for the implementation of this product on a module board.
- ■ Decoupling capacitors of 120pF, 10nF & 1µF ±10% are recommended for all DC access.
- ■ See application note AN0017 for more details.

Note: All board measurements are performed using **shielded cables, even for DC bias**, **to ensure safe operation**.



Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard technics involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 available at http://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Description of Evaluation Board

Refer to the application note AN0031 available at https://www.ums-rf.com for the description of Evaluation Board for Packaged Die and recommendations for this UMS package product.

Ordering request reference

Package: CHA4262-QDG/XY
Stick: XY = 20 Tape & reel: XY = 21