

## 27 - 31 GHz 5W High Power Amplifier

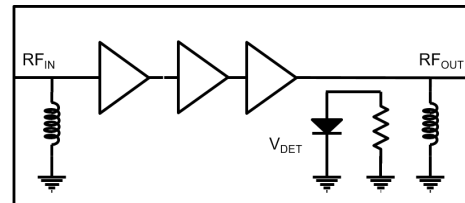
### GaN Monolithic Microwave IC

#### Description

The CHA6357-98F is a bare die three-stage GaN Power Amplifier operating between 27GHz and 31GHz. This amplifier typically provides 5W of saturated Output Power associated to 23% and 24dB of Power Gain. This amplifier exhibits 33dBm Linear Power with -30dBc ACPR and 27dB Gain. In addition, the CHA6357 provides high linearity with a low consumption when operated with output power back-off. It therefore can be used as a Driver of HPA.

The component is internally matched to 50Ω at both the input and output. It integrates output power detector and ESD RF protection. It is manufactured on a robust GaN-on-SiC HEMT process.

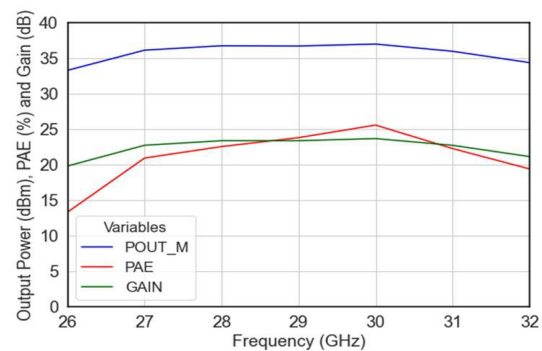
It is well suited for VSAT, SatCom uplink, 5G communication and Radio links applications.



#### Main Features

- Broadband performances: 27-31GHz
- 30dB of small signal gain
- 37dBm Pout for +14dBm Input power
- >35 dBc ACPR at 26dBm Output power <sup>(1)</sup>
- 23% PAE at 37dBm Output power
- DC bias: Vd=25V@Idq=140mA
- Output Power detector included
- Chip size: 2.5 x 1.6mm<sup>2</sup>
- Available as bare die

<sup>(1)</sup> 30MHz Modulation Bandwidth, 8PSK



Output Power [dBm] PAE [%] & Gain [dB] at Pin=14dBm & T<sub>backside</sub>=25°C

#### Main Electrical Characteristics

T<sub>backside</sub> = +25°C (T<sub>backside</sub> : Die backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27		31	GHz
Gain	Linear Gain		30		dB
Psat	Saturated Output Power		37		dBm
PAE	Power Added Efficiency		23		%
ACPR	ACPR at Pout = 33dBm with 8PSK (30MHz Modulation Bandwidth)		-30		dBc

## Specifications

$T_{\text{backside}} = +25^{\circ}\text{C}$ ,  $V_d = +25\text{V}$

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27		31	GHz
Gain	Linear Gain		30		dB
Psat	Saturated Output Power ( $P_{\text{in}} = 14\text{dBm}$ )		37		dBm
PAE	Power Added Efficiency		23		%
S11	Input Return Loss		-13		dB
S22	Output Return Loss		-15		dB
ACPR	ACPR at $P_{\text{out}} = 33\text{dBm}$ with 8PSK (30MHz Modulation Bandwidth)		-30		dBc
Vdetect	Voltage detection $V_{\text{REF}} - V_{\text{DET}}$ up to $P_{\text{sat}}$		10 to 1200		mV
Idq	Total quiescent drain current		140		mA
Vc	Detector bias voltage		5		V

These values are representative of on-board measurements as defined on the drawing in paragraph "Evaluation board".

## Absolute Maximum Ratings<sup>(1)</sup>

$T_{\text{backside}} = +25^{\circ}\text{C}$

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Vg	Gate bias voltage	-7 to -1	V
Pin	Maximum peak input power overdrive	18	dBm

<sup>(1)</sup> Operation of this device above anyone of these parameters may cause permanent damage.

## Recommended Operating Range<sup>(2), (3)</sup>

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	20 to 25	V
Vg	Gate bias voltage	-5 to -2.5	V
Vc	Detector bias voltage	5	V
Idq	Total Quiescent Drain Current	75 to 140	mA
Pin	Input Power	14	dBm
Tj	Maximum Junction temperature <sup>(4)</sup>	200	$^{\circ}\text{C}$

<sup>(2)</sup> Electrical performances are defined for specified test conditions

<sup>(3)</sup> Electrical performances are not guaranteed over all recommended operating conditions

<sup>(4)</sup> See Device thermal performances section

## Temperature Range

$T_{\text{backside}}$	Operating temperature range	-40 to +85	$^{\circ}\text{C}$
Tstg	Storage temperature range	-55 to +150	$^{\circ}\text{C}$

**Typical Bias Conditions** $T_{\text{backside}} = +25^{\circ}\text{C}$ 

Symbol	Pad N°	Parameter	Values	Unit
G1	3	Stage 1 Gate Supply	-5 to -1	V
G2	5	Stage 2 Gate Supply	-5 to -1	V
G3S	9	Stage 3 South Gate Supply	-5 to -1	V
G3N	18	Stage 3 North Gate Supply	-5 to -1	V
D1	22	Stage 1 Drain Supply	20 to 25	V
D2S	7	Stage 2 South Drain Supply	20 to 25	V
D2N	20	Stage 2 North Drain Supply	20 to 25	V
D3S	11	Stage 3 Drain Supply	20 to 25	V
VC	16	Detector Supply	5	V
REF	17	Detector reference voltage		V
DET	15	Detector detected voltage		V

**“Power ON” sequence**

1. Bias HPA gate voltage at  $V_g$  close to  $V_{\text{pinch-off}}$  ( $V_g \sim -5\text{V}$ )
2. Set  $V_d$  bias voltage to 0V:  $I_d = 0\text{mA}$
3. Apply  $V_d$  bias voltage,  $V_d = 25\text{V}$ :  $I_d = 0\text{mA}$
4. Set  $V_c$  bias voltage to 5V for Detector biasing
5. Increase  $V_g$  up to quiescent bias drain current  $I_{dq}$
6. Apply RF input Power

**“Power OFF” sequence**

1. Turn off RF input power
2. Bias HPA Gate voltage at  $V_g \sim -5\text{V}$ :  $I_d = 0\text{mA}$
3. Decrease  $V_d$  bias voltage down to 0V
4. Set  $V_c$  bias voltage to 0V
5. Turn  $V_g$  bias voltage to 0V

## Device thermal performance

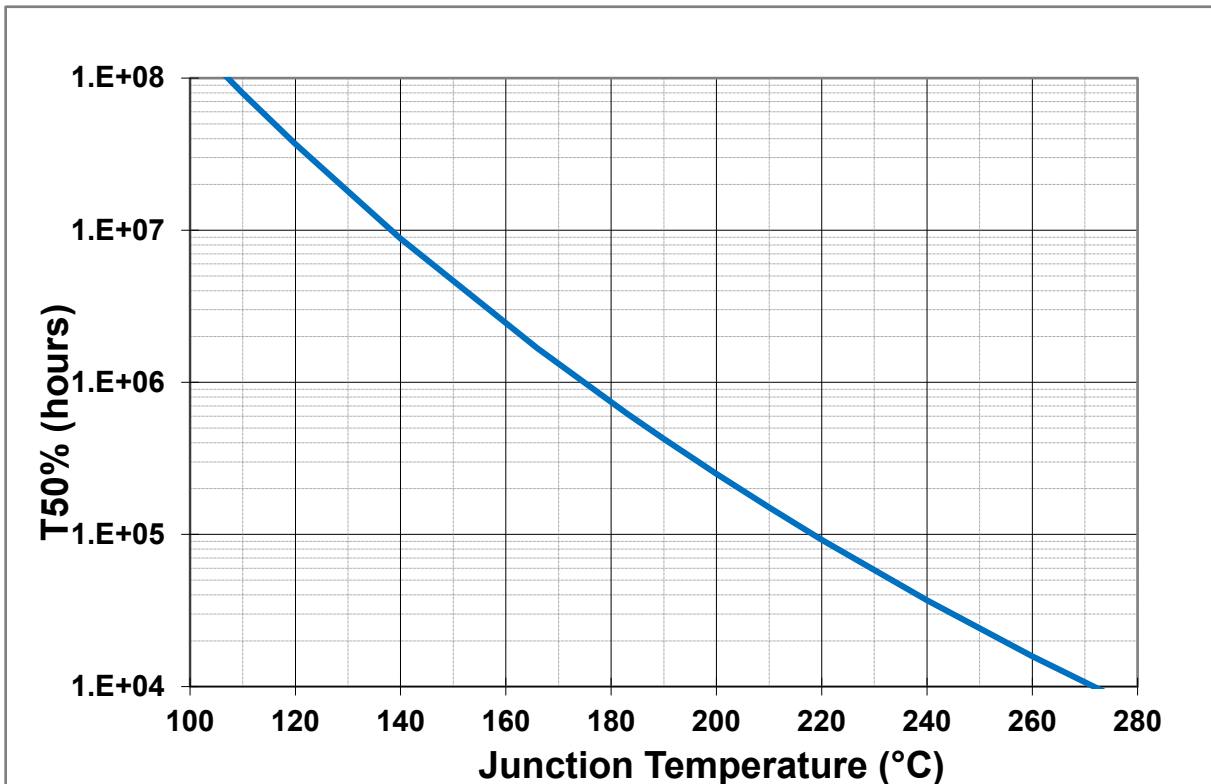
All the figures given in this section are obtained assuming that the chip backside is only cooled down by conduction through the test board (no convection mode considered).

The temperature is monitored at the chip backside ( $T_{backside}$ ).

The system maximum temperature must be adjusted in order to guarantee that  $T_{junction}$  remains below the maximum value specified in the Recommended Operating Rating table. The system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	$T_{junction}$ (°C)	$R_{TH}$ (°C/W)	$T_{50}$ (hours)
$R_{TH}^{(1)}$ Thermal Resistance (Junction to Backside)	Vd=25V Pout=35.5dBm Pdiss=12W	186	8.47	5E+05
$R_{TH}^{(1)}$ Thermal Resistance (Junction to Backside)	Vd=25V Pout=18dBm Pdiss=3.4W	115	8.85	5E+07

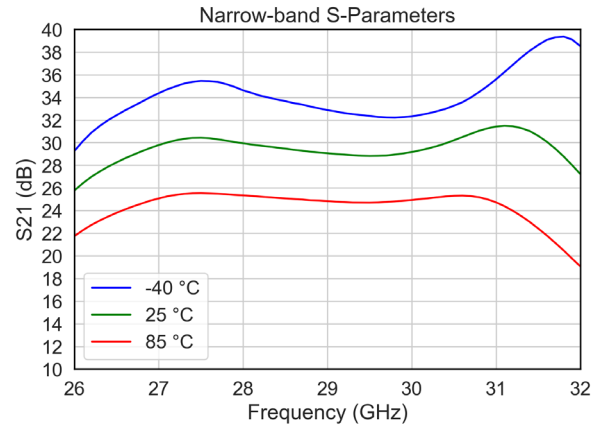
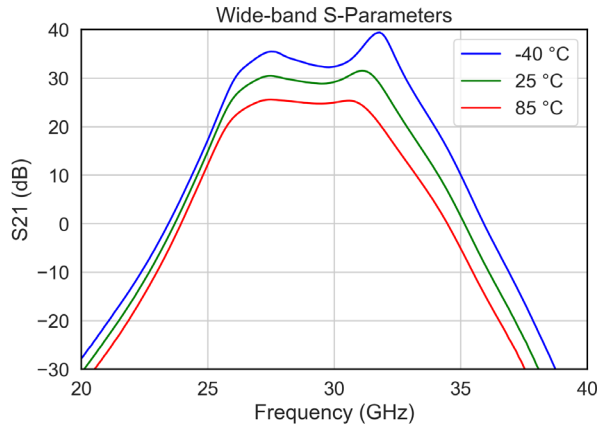
<sup>(1)</sup> Assuming 85°C  $T_{backside}$



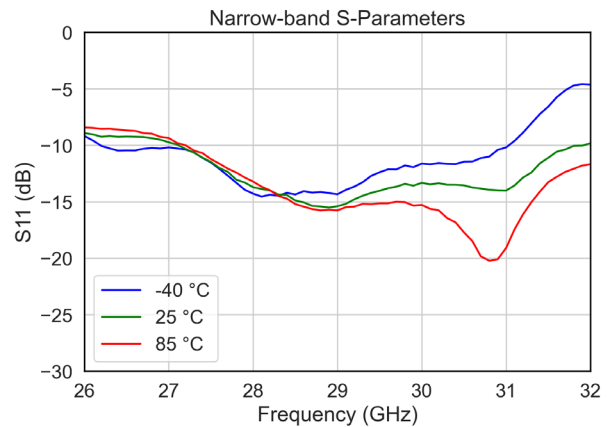
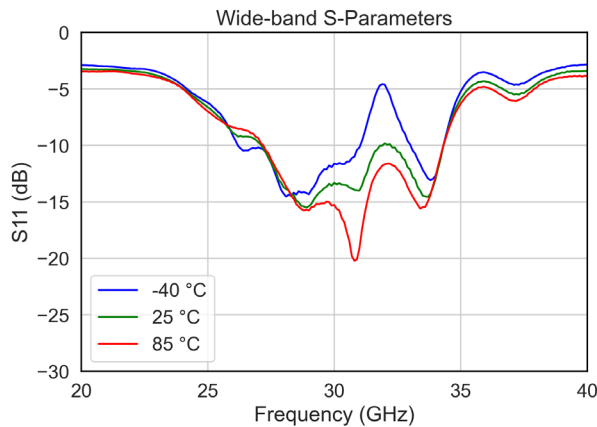
**Typical Board Measurements : S-Parameters**

**Test conditions :** CW,  $V_d = +25V$ ,  $I_{dq} = 140mA$ ,  $T_{backside} = -40^{\circ}C / 25^{\circ}C / 85^{\circ}C$

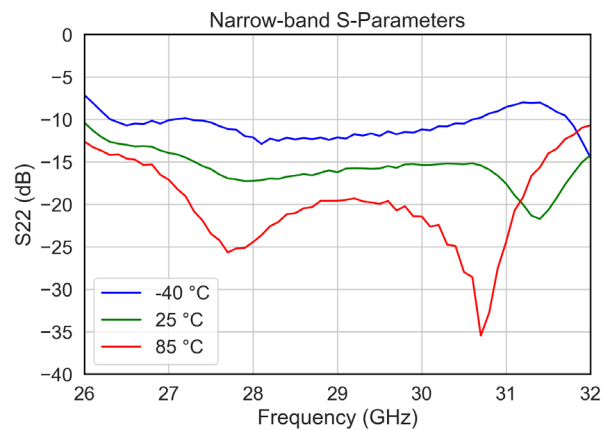
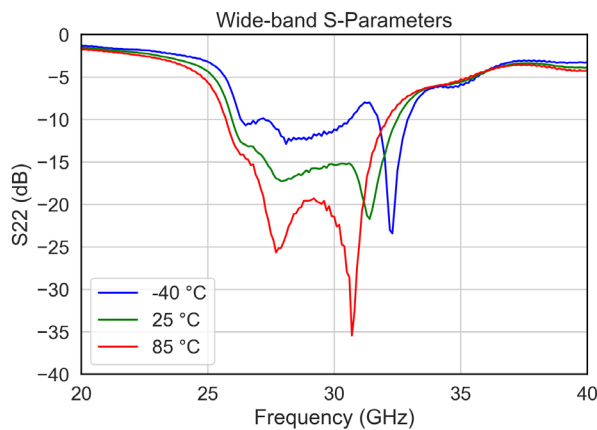
**Linear Gain vs. Frequency & Temperature**



**Input Return Loss vs. Frequency & Temperature**



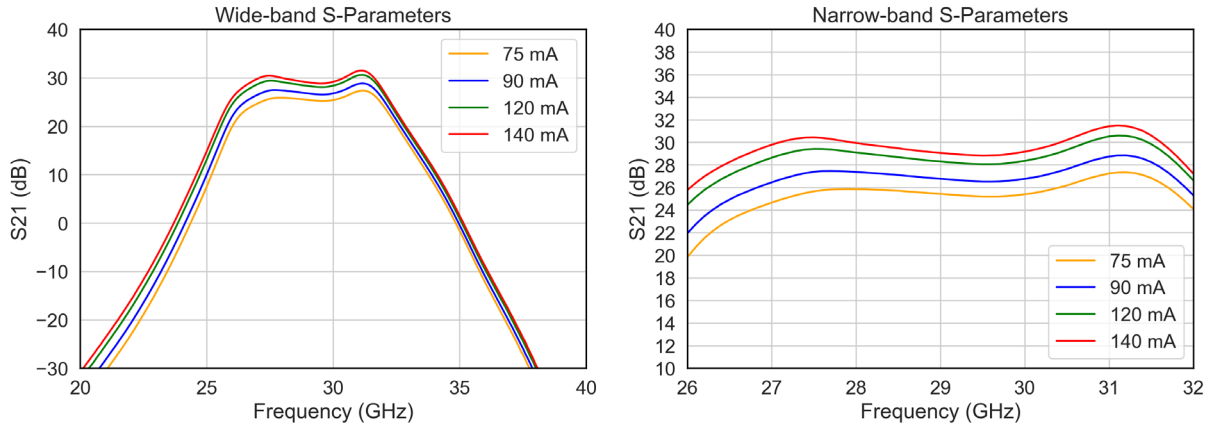
**Output Return Loss vs. Frequency & Temperature**



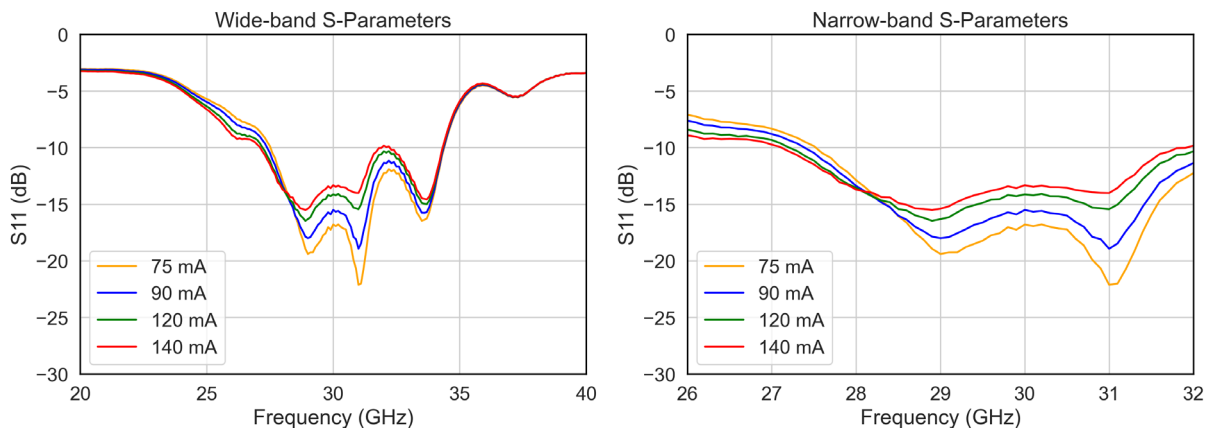
## Typical Board Measurements : S-Parameters

Test conditions : CW,  $V_d = +25V$ ,  $I_{dq} = 75/90/120/140mA$ ,  $T_{backside} = 25^\circ C$

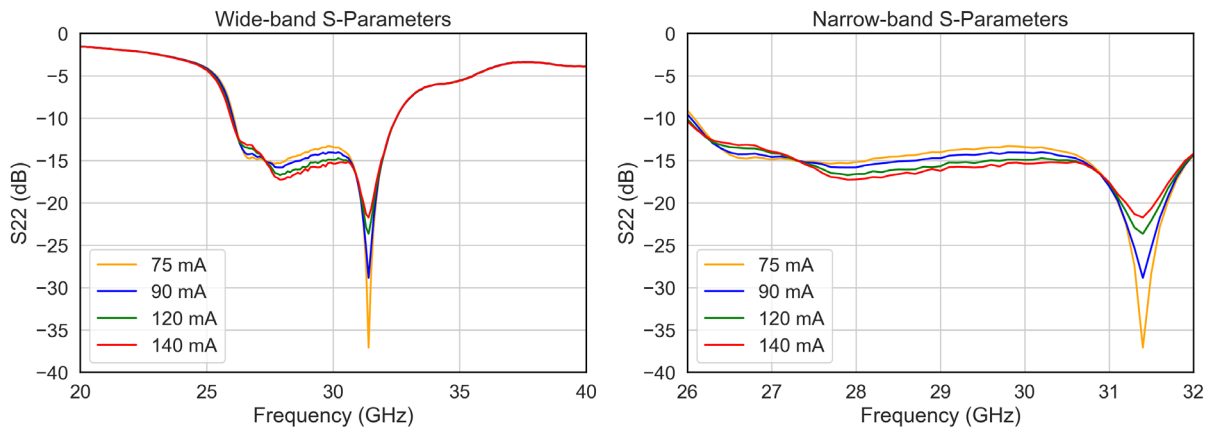
### Linear Gain vs. Frequency & Idq



### Input Return Loss vs. Frequency & Idq



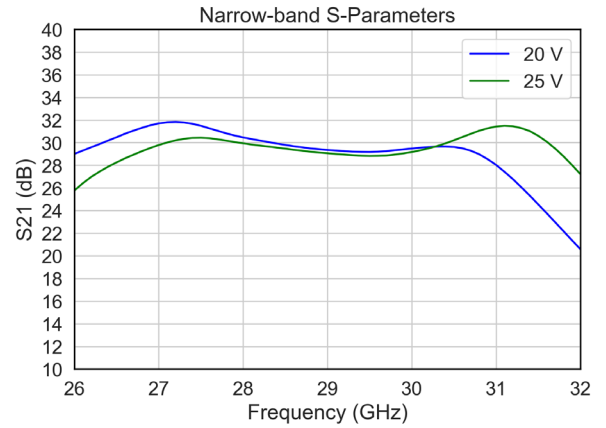
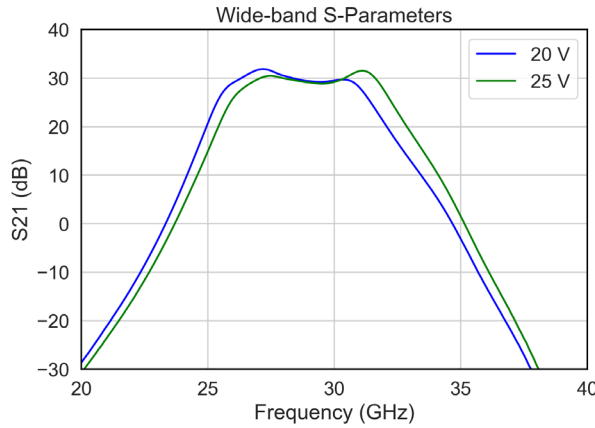
### Output Return Loss vs. Frequency & Idq



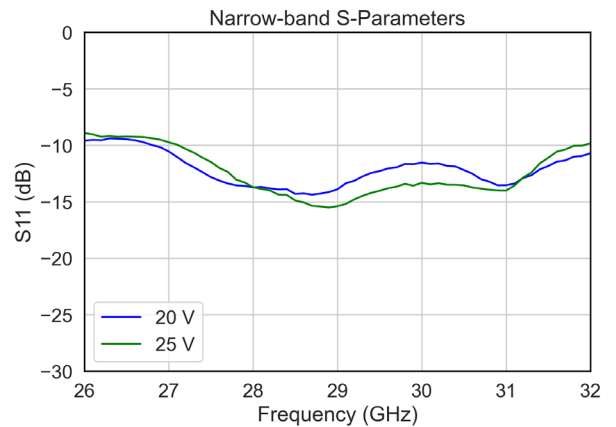
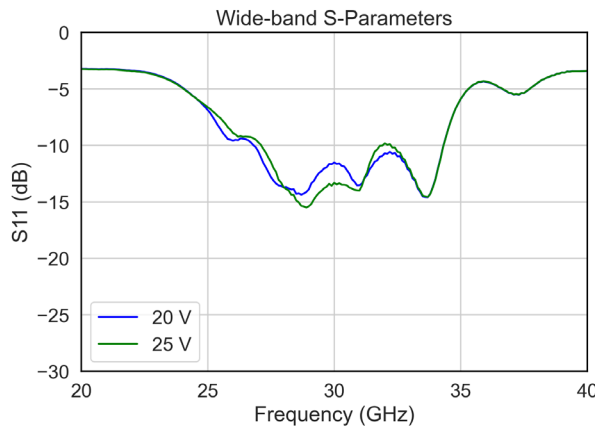
**Typical Board Measurements : S-Parameters**

**Test conditions :** CW,  $V_d = +20/+25V$ ,  $I_{dq} = 140mA$ ,  $T_{backside} = 25^{\circ}C$

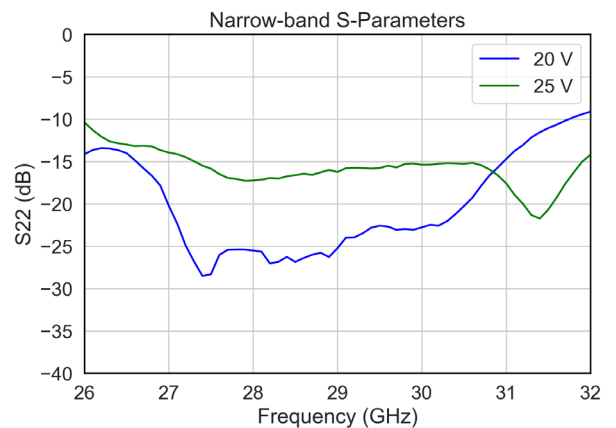
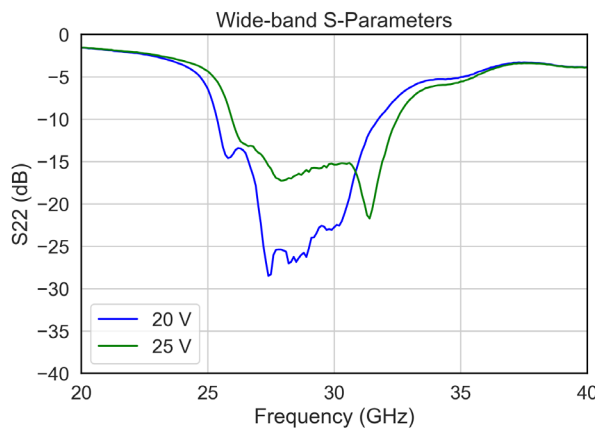
**Linear Gain vs. Frequency &  $V_d$**



**Input Return Loss vs. Frequency &  $V_d$**



**Output Return Loss vs. Frequency &  $V_d$**

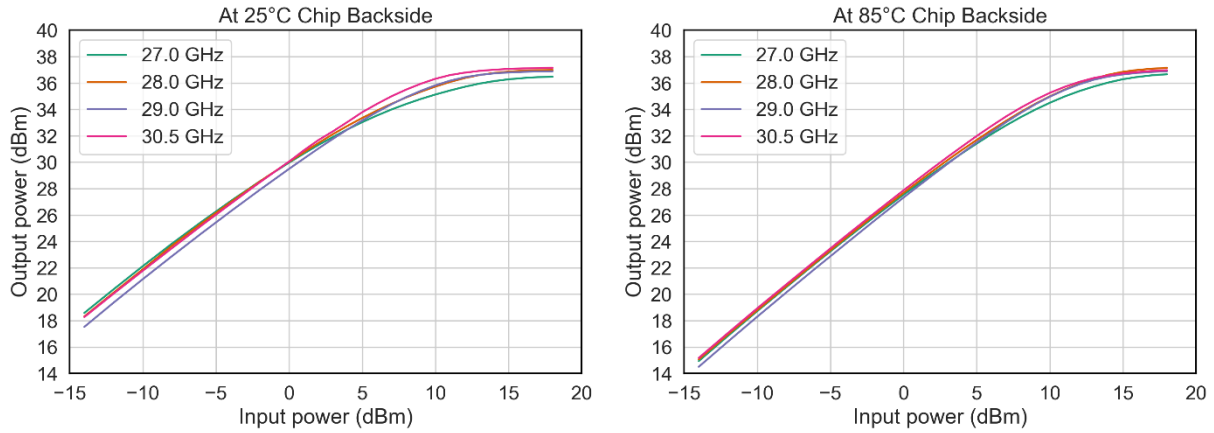


## Typical Board Measurements : Large Signal

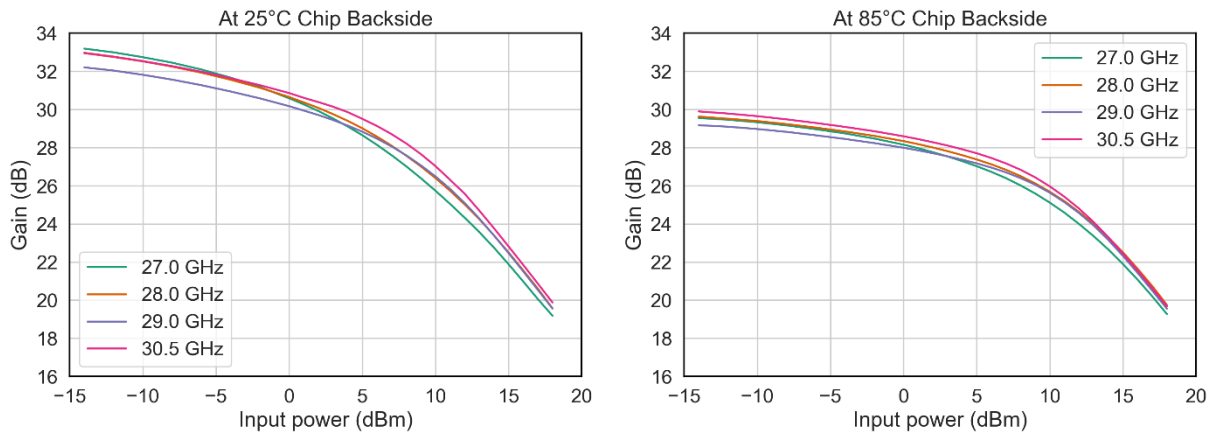
Test conditions : CW,  $V_d = +25V$ ,  $I_{dq} = 140mA$ ,  $T_{backside} = 25^\circ C / 85^\circ C$

Board losses are de-embedded. Measurements are given in the die access plans.

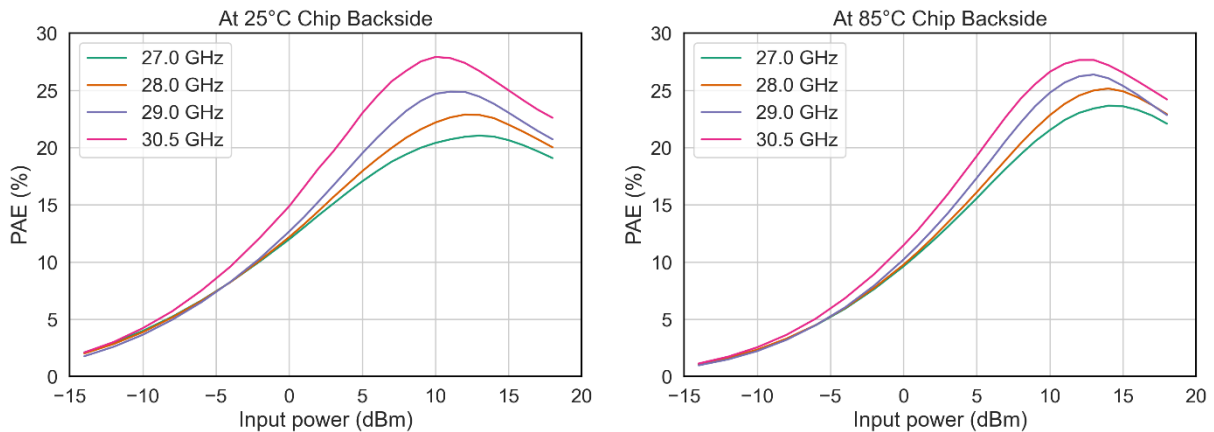
### Output Power vs. Input Power & Frequency



### Gain vs. Input Power & Frequency



### PAE vs. Input Power & Frequency

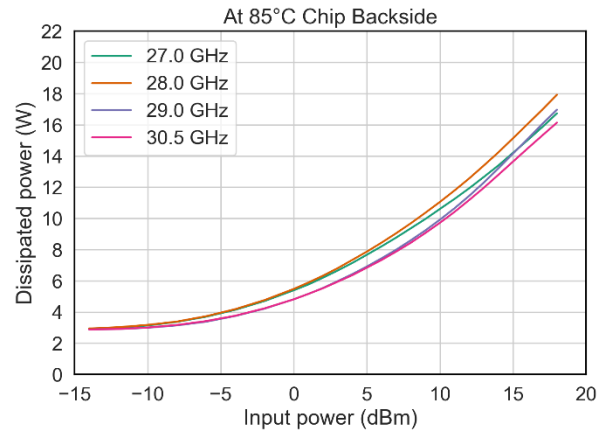
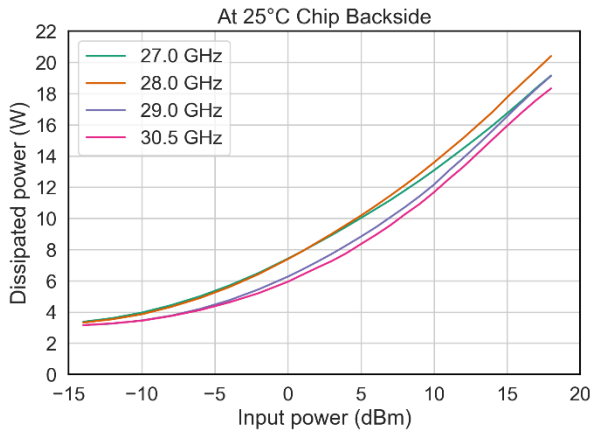


**Typical Board Measurements : Large Signal Performance**

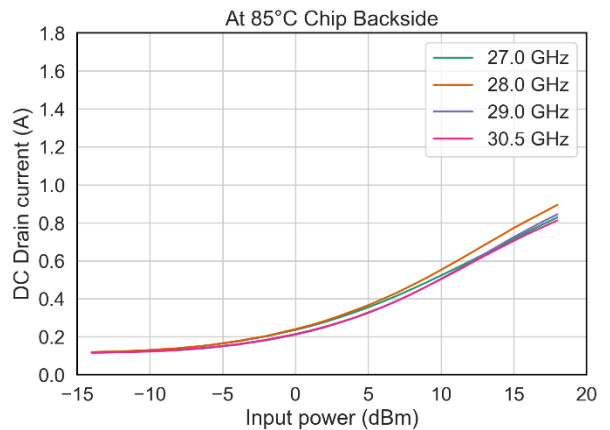
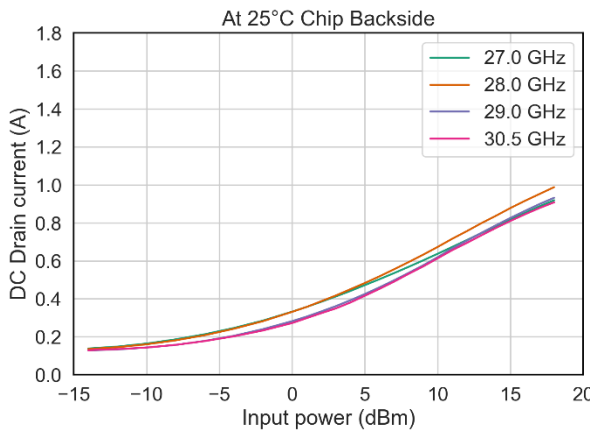
**Test conditions :** CW,  $V_d = +25V$ ,  $I_{dq} = 140mA$ ,  $T_{backside} = 25^\circ C / 85^\circ C$

Board losses are de-embedded. Measurements are given in the die access plans.

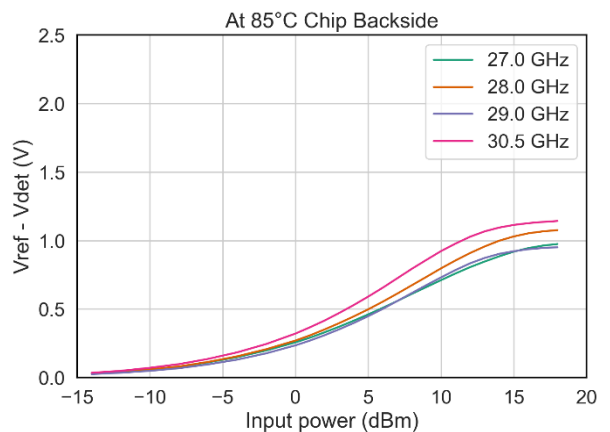
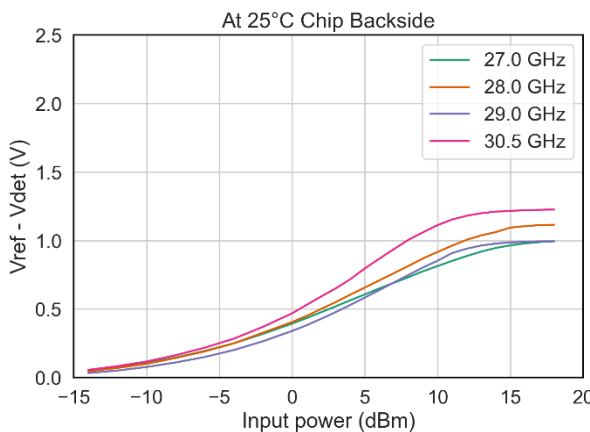
**Dissipated Power vs. Input Power and Frequency**



**Drain Current vs. Input Power and Frequency**



**Power Detector Voltage vs. Input Power and Frequency**

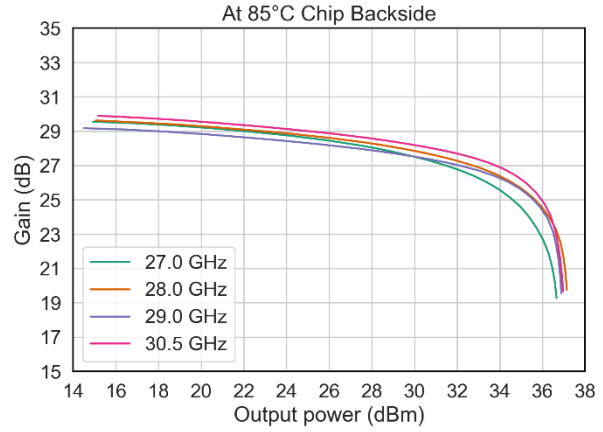
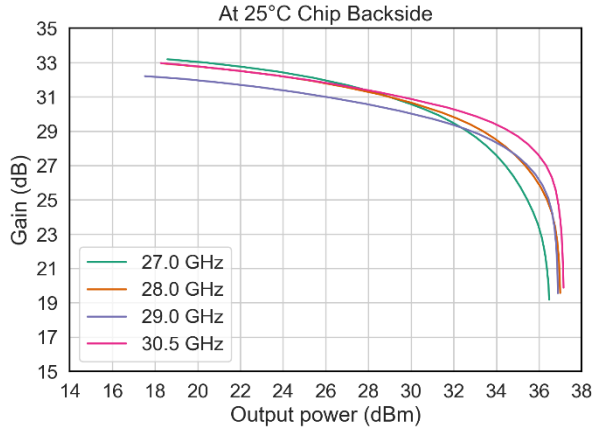


## Typical Board Measurements : Large Signal Performance

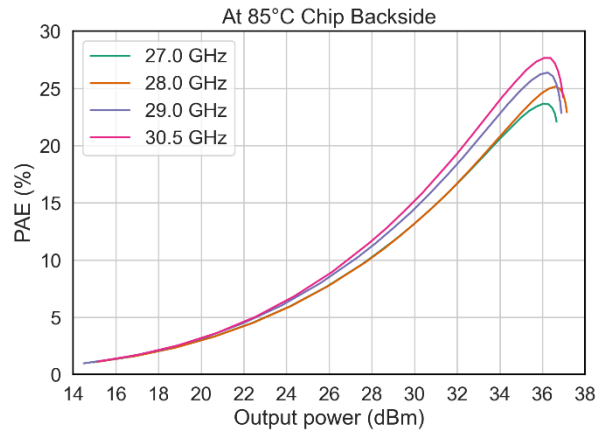
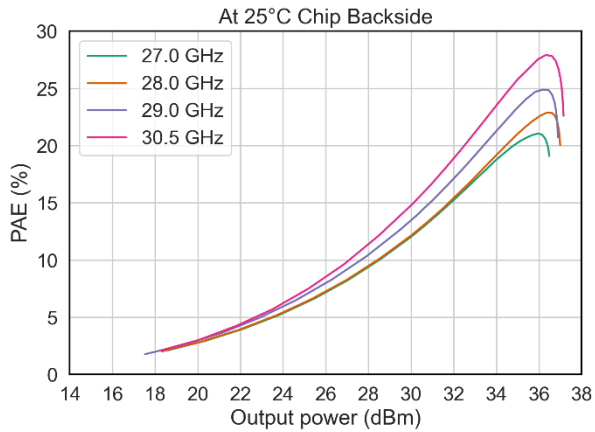
**Test conditions :** CW,  $V_d = +25V$ ,  $I_{dq} = 140mA$ ,  $T_{backside} = 25^\circ C / 85^\circ C$

Board losses are de-embedded. Measurements are given in the die access plans.

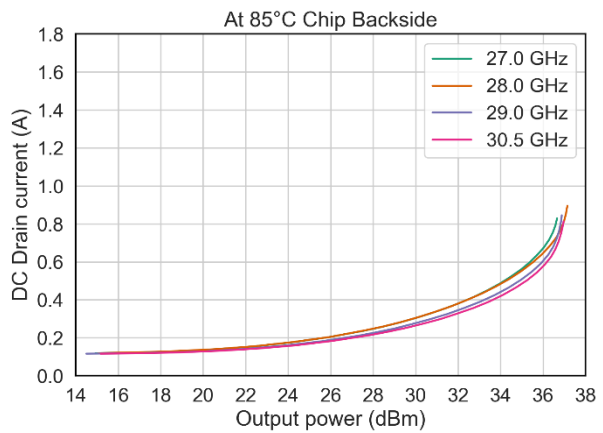
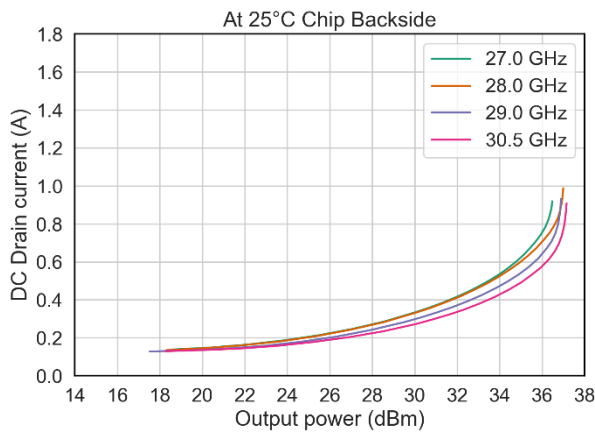
### Gain vs. Output Power & Frequency



### Power Added Efficiency vs. Output Power & Frequency



### Drain Current vs. Output Power & Frequency

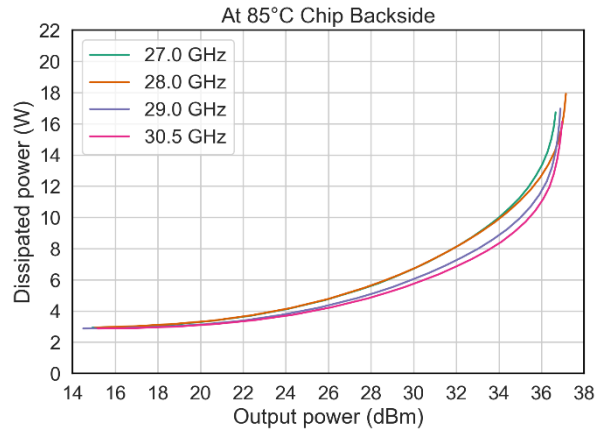
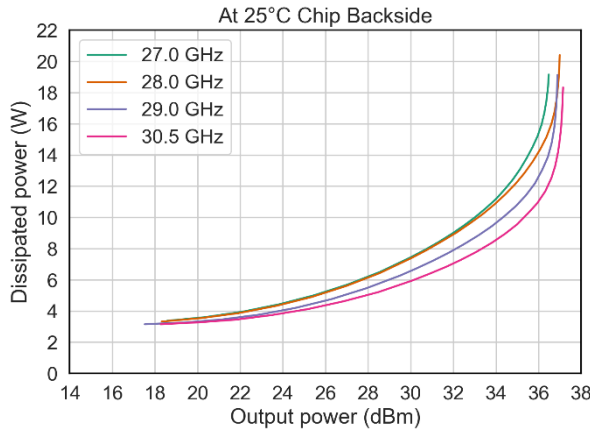


**Typical Board Measurements : Large Signal Performance**

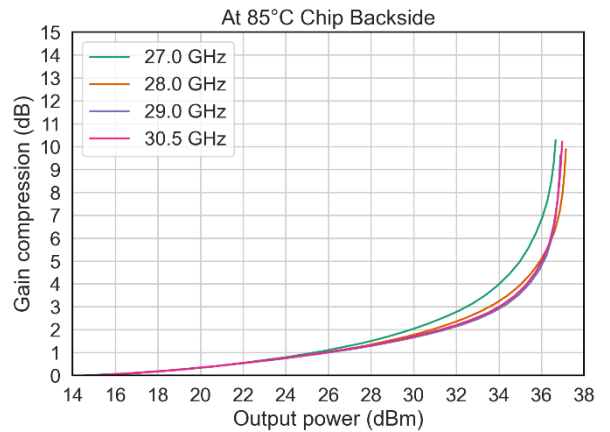
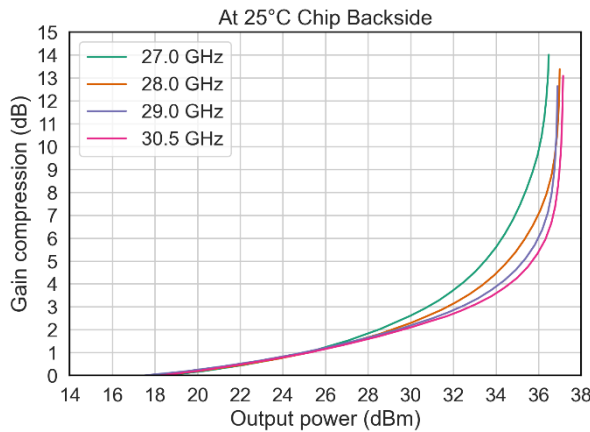
**Test conditions :** CW,  $V_d = +25V$ ,  $I_{dq} = 140mA$ ,  $T_{backside} = 25^\circ C / 85^\circ C$

Board losses are de-embedded. Measurements are given in the die access plans.

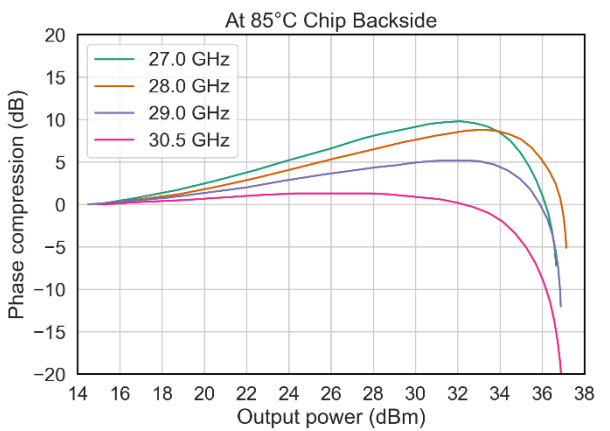
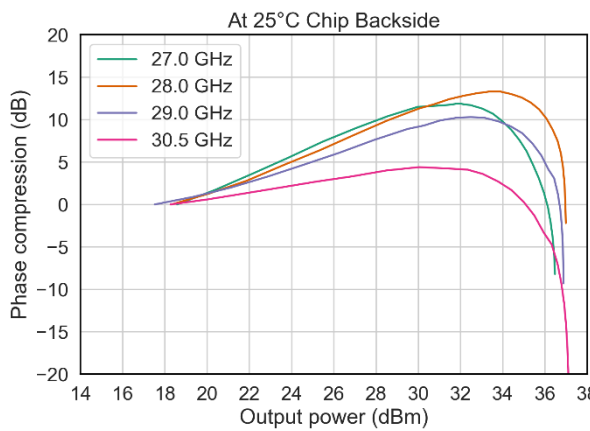
**Dissipated Power vs. Output Power & Frequency**



**Gain Compression vs. Output Power & Frequency**



**Phase Compression vs. Output Power & Frequency**

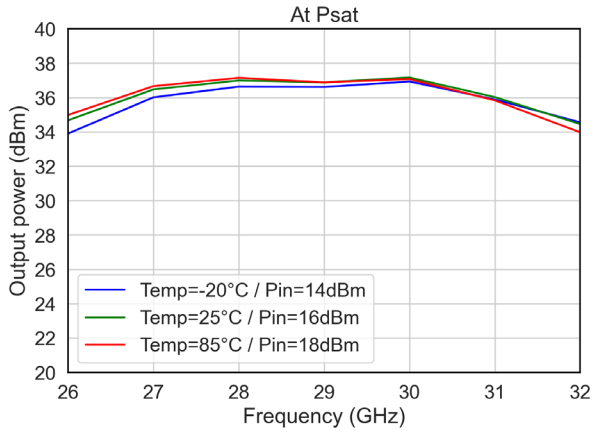
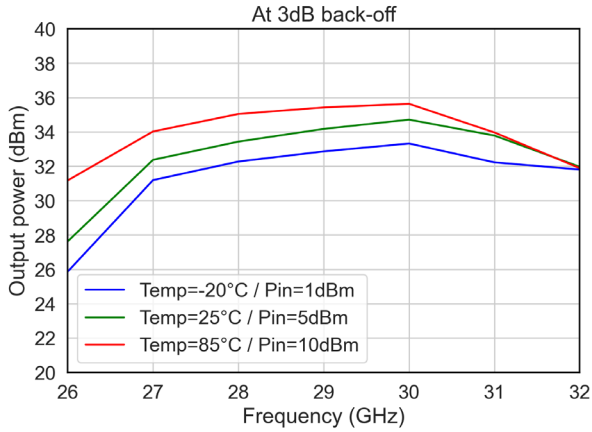


## Typical Board Measurements : Large Signal Performance

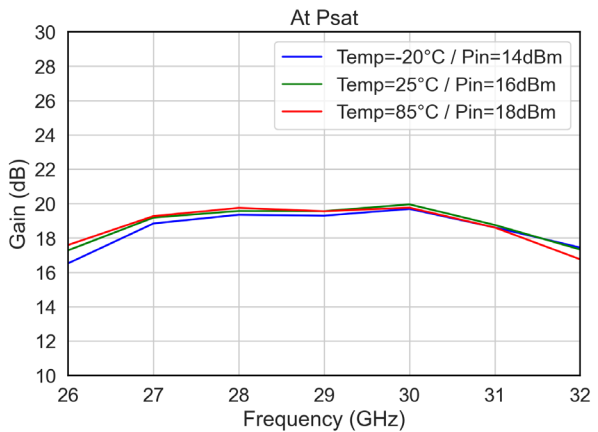
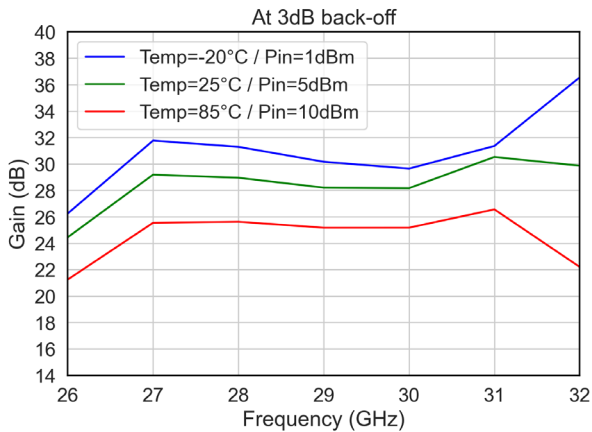
Test conditions : CW, Vd = +25V, Idq = 140mA, T<sub>backside</sub> = -20°C / 25°C / 85°C

Board losses are de-embedded. Measurements are given in the die access plans

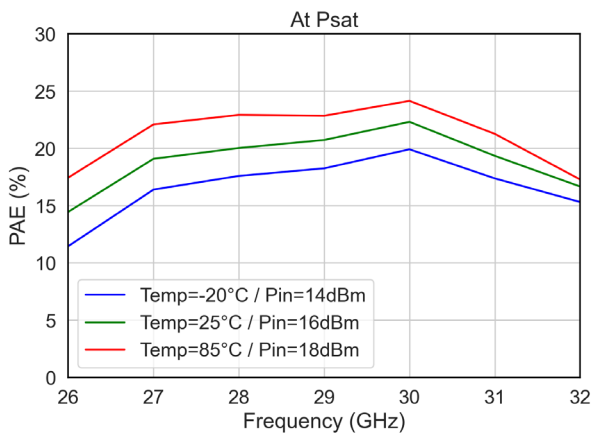
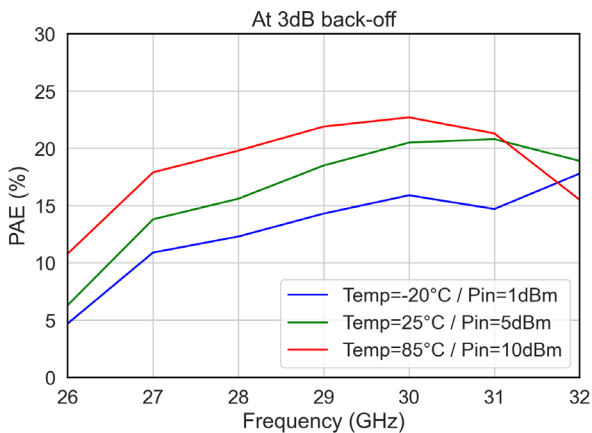
### Output Power vs. Frequency & Temperature



### Gain vs. Frequency & Temperature



### Power Added Efficiency vs. Frequency & Temperature

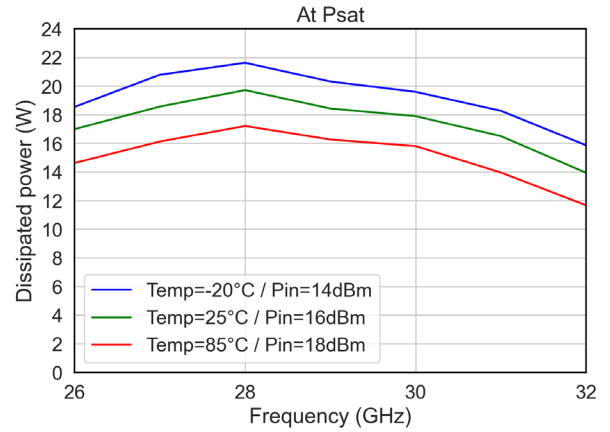
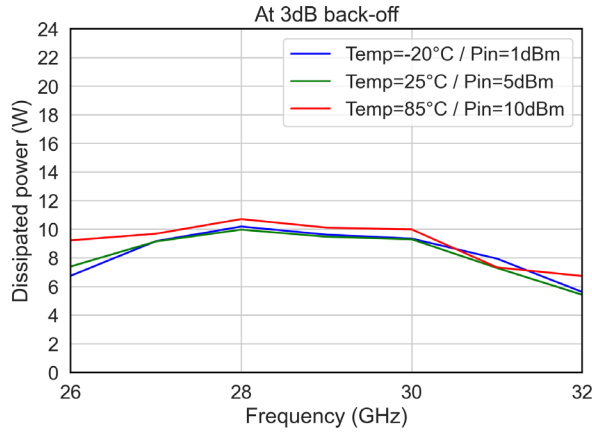


**Typical Board Measurements : Large Signal Performance**

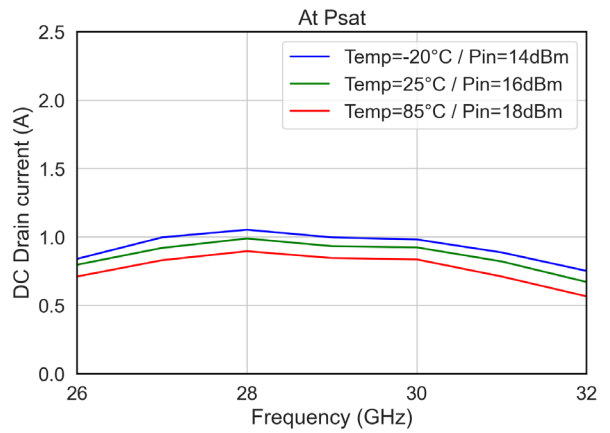
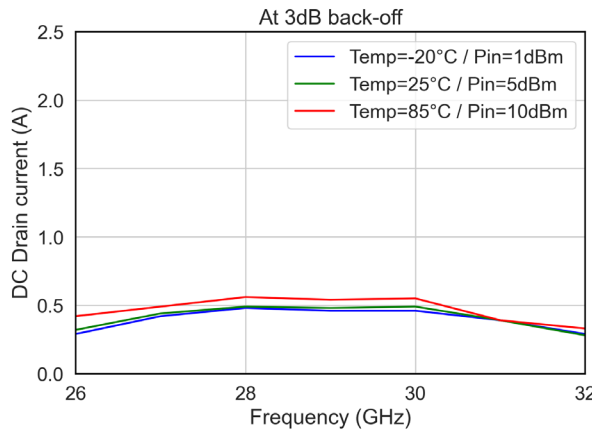
**Test conditions :** CW,  $V_d = +25V$ ,  $I_{dq} = 140mA$ ,  $T_{backside} = -20^{\circ}C / 25^{\circ}C / 85^{\circ}C$

Board losses are de-embedded. Measurements are given in the die access plans.

**Dissipated Power vs. Frequency & Temperature**



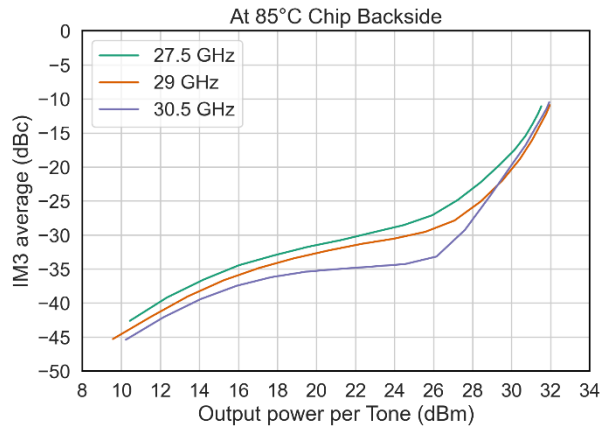
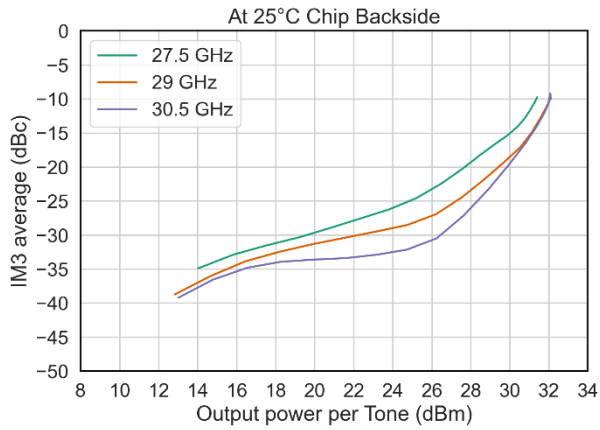
**Drain Current vs. Frequency & Temperature**



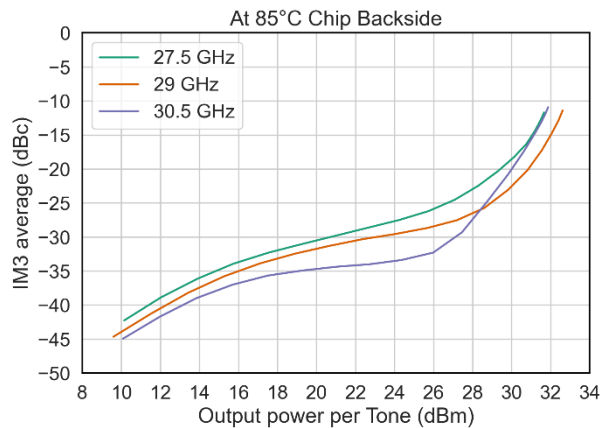
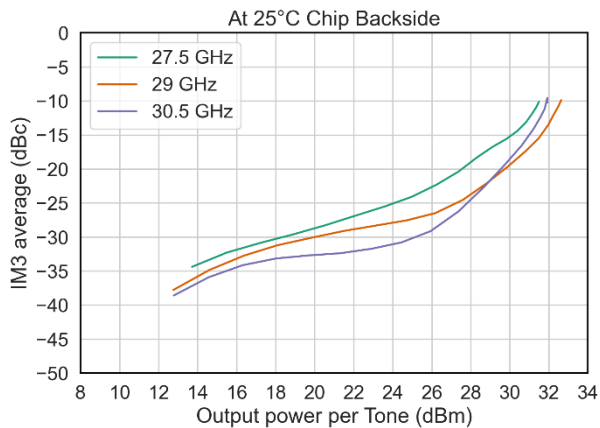
## Typical Board Measurements : Linearity – IMD3

**Test conditions :** CW dual tones,  $V_d = +25V$ ,  $I_{dq} = 140mA$ ,  $T_{backside} = +25^{\circ}C/85^{\circ}C$   
 Board losses are de-embedded. Measurements are given in the die access plans

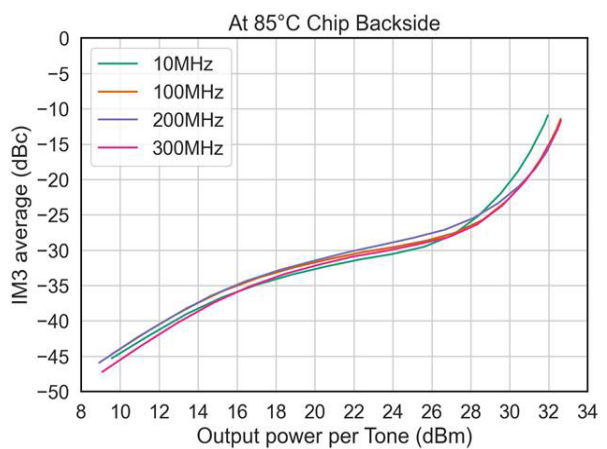
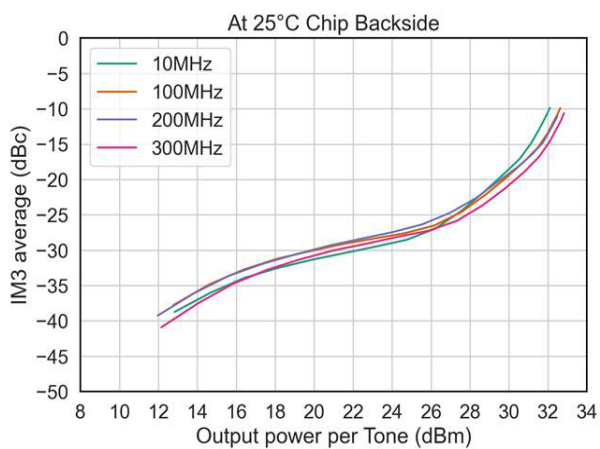
### IMD3 vs. Output Power per Tone & Frequency at $\Delta f = 10MHz$



### IMD3 vs. Output Power per Tone & Frequency at $\Delta f = 100MHz$



### IMD3 vs. Output Power per Tone & Tone spacing at $F_c = 29GHz$

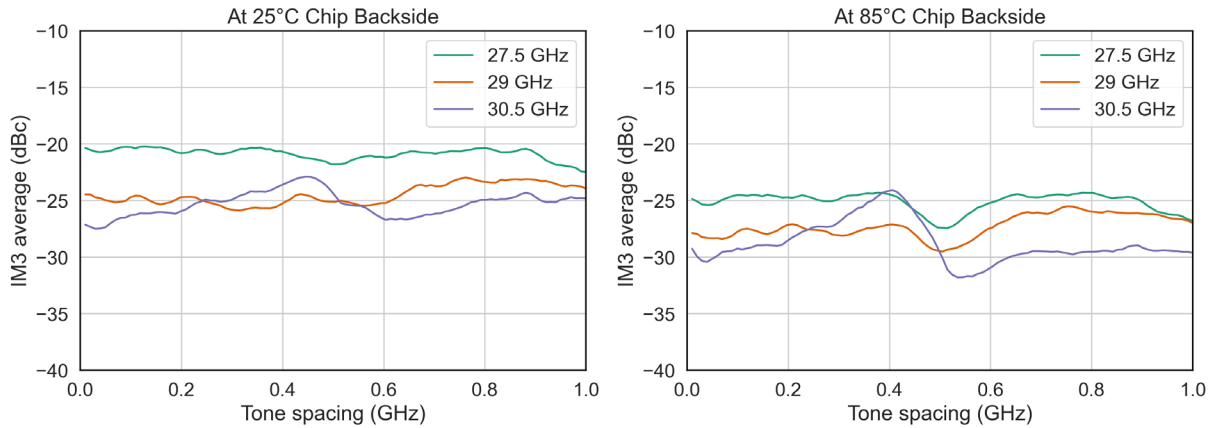


**Typical Board Measurements: Linearity – IMD3**

**Test conditions :** CW dual tones, Vd = +25V, Idq = 140mA, Pout/tone = 28dBm,  
 T<sub>backside</sub> = +25°C/85°C

Board losses are de-embedded. Measurements are given in the die access plans.

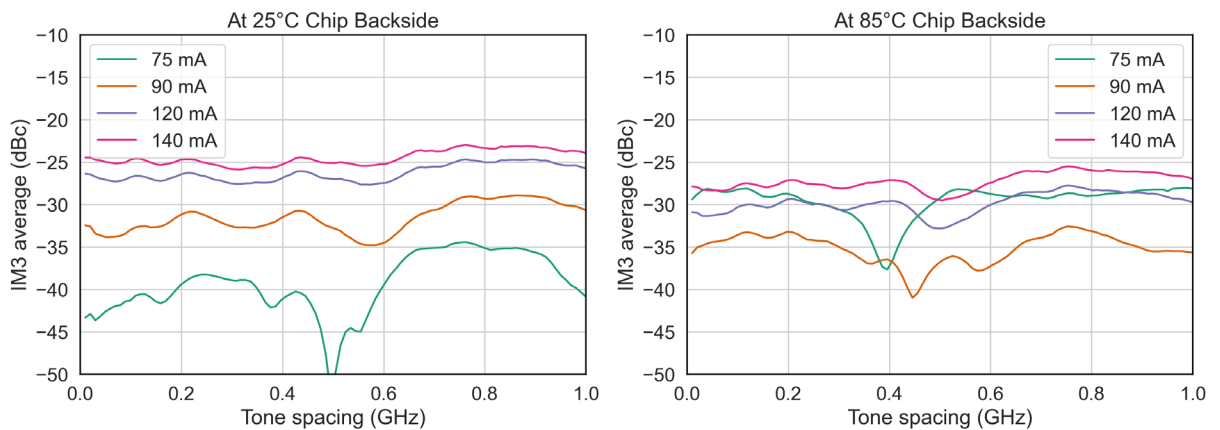
**IMD3 vs. Tone Spacing & Frequency**



**Test conditions :** CW dual tones, Vd = +25V, Fc = 29 GHz, Pout/tone = 28dBm,  
 T<sub>backside</sub> = +25°C/85°C

Board losses are de-embedded. Measurements are given in the die access plans.

**IMD3 vs. Tone Spacing & Drain Current**

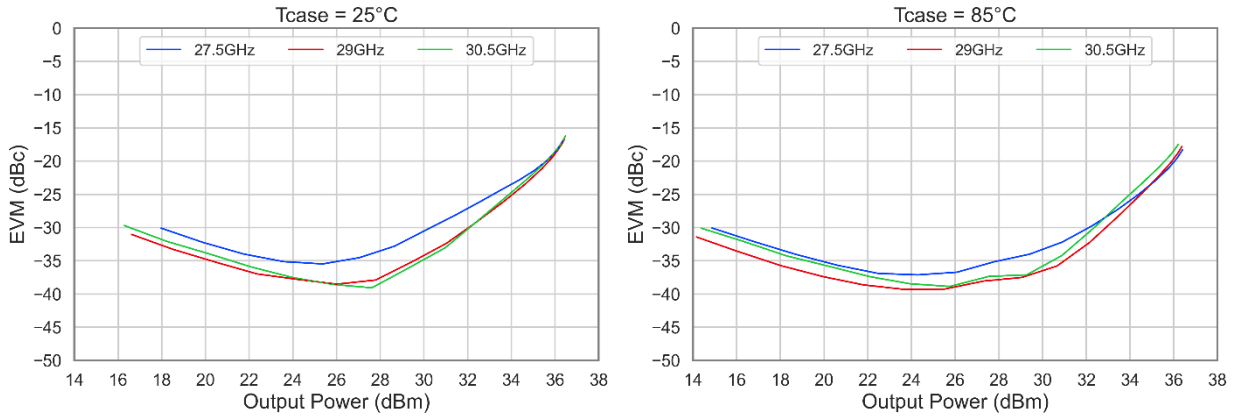


## Typical Board Measurements: Linearity – Modulated Signals

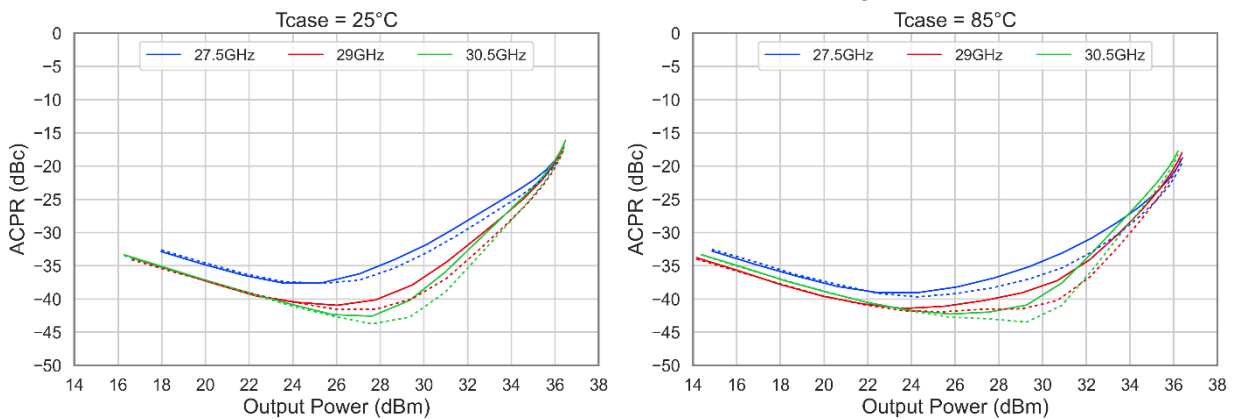
**Test conditions :** Modulated signal,  $V_d = +25V$ ,  $I_{dq} = 140mA$ ,  $T_{backside} = 25^\circ C / 85^\circ C$ , **8PSK**, **BW = 30 MHz**, Roll-off = 0.2, PAPR=5dB

Board losses are de-embedded. Measurements are given in the die access plans.

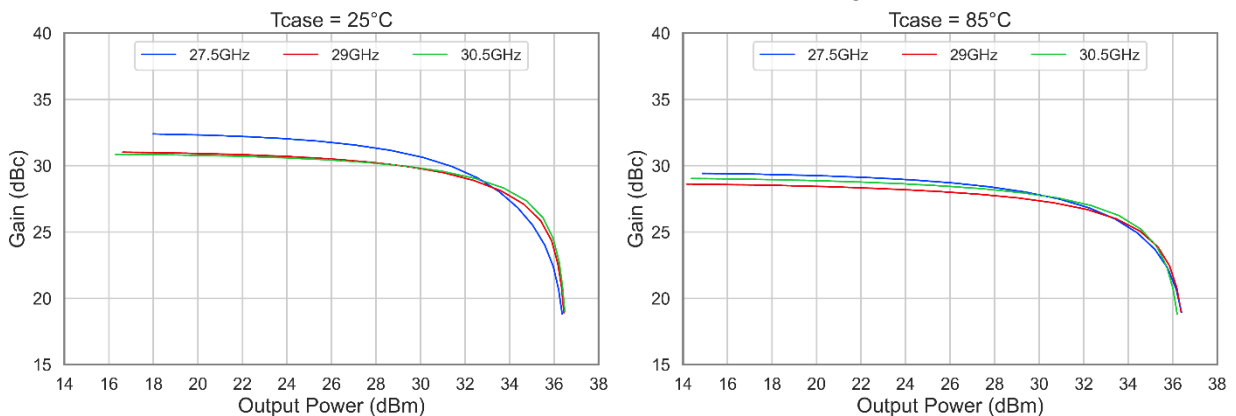
### EVM vs. Output Power & Frequency



### ACPR vs. Output Power & Frequency



### Gain vs. Output Power & Frequency

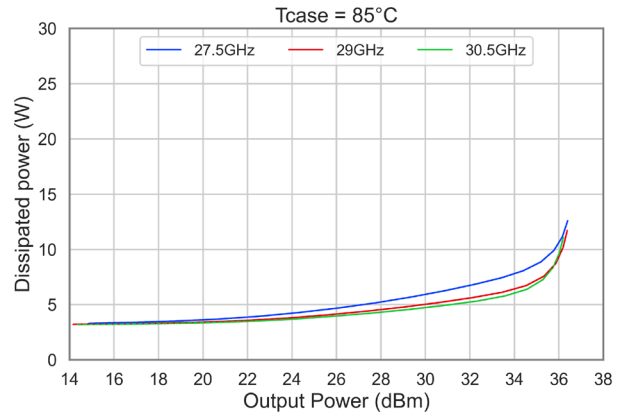
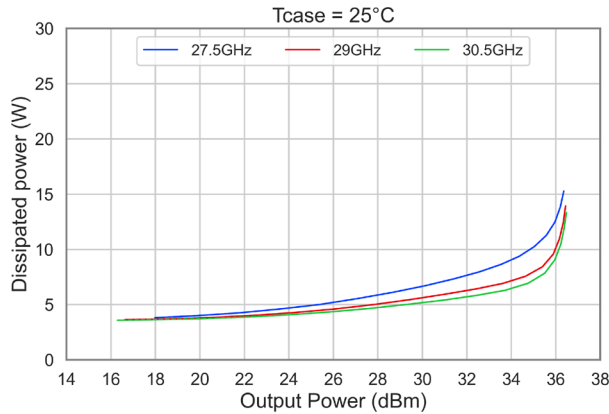


**Typical Board Measurements: Linearity – Modulated Signals**

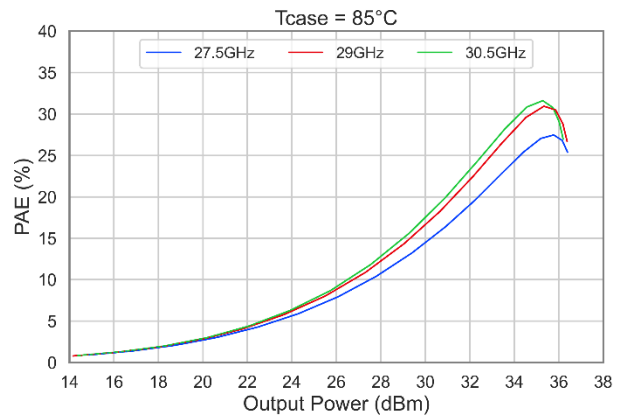
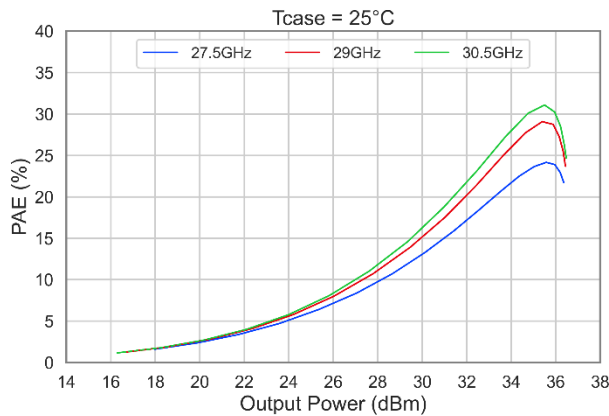
**Test conditions :** Modulated signal,  $V_d = +25V$ ,  $I_{dq} = 140mA$ ,  $T_{backside} = 25^\circ C / 85^\circ C$ , **8PSK**, **BW = 30 MHz**, Roll-off = 0.2, PAPR=5dB

Board losses are de-embedded. Measurements are given in the die access plans.

**Dissipated Power vs. Output Power & Frequency**



**PAE vs. Output Power & Frequency**

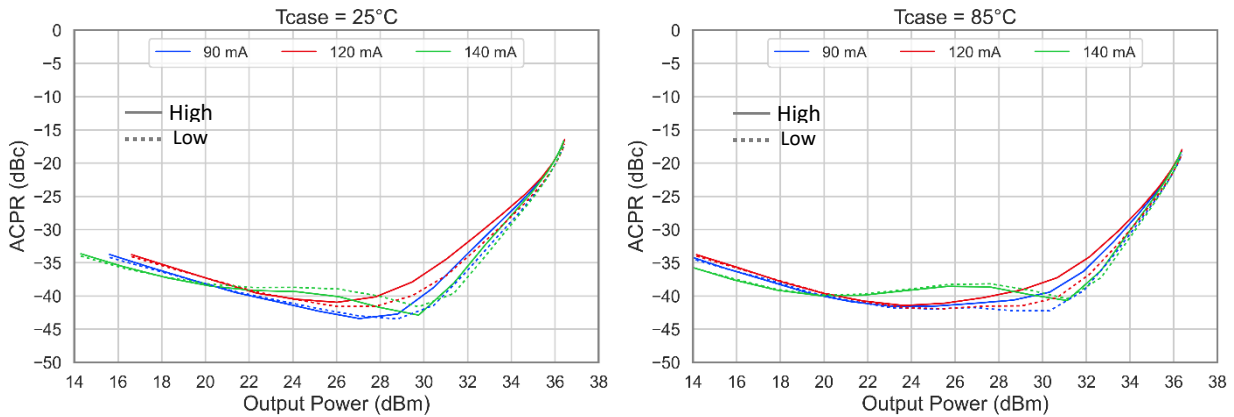


## Typical Board Measurements: Linearity – Modulated Signals

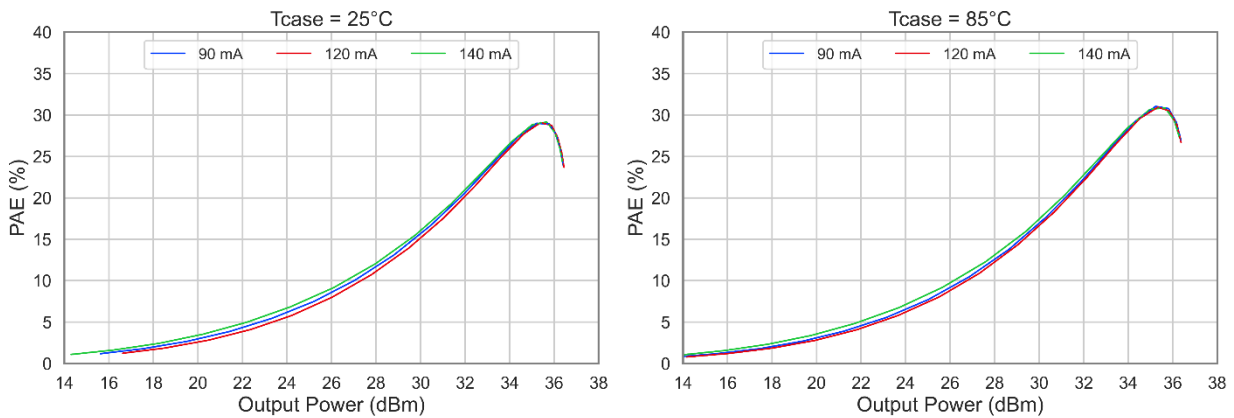
**Test conditions :** Modulated signal,  $V_d = +25V$ ,  $Freq = 29\text{ GHz}$ ,  $T_{backside} = 25^\circ\text{C} / 85^\circ\text{C}$ , **8PSK**, **BW = 30 MHz**, Roll-off = 0.2, PAPR=5dB

Board losses are de-embedded. Measurements are given in the die access plans.

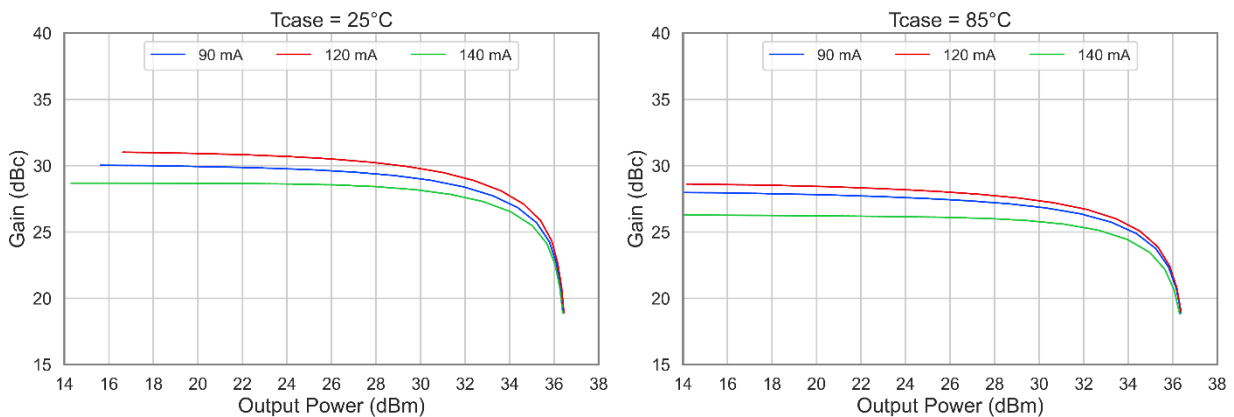
### ACPR vs. Output Power & Idq



### PAE vs. Output Power & Idq



### Gain vs. Output Power & Idq

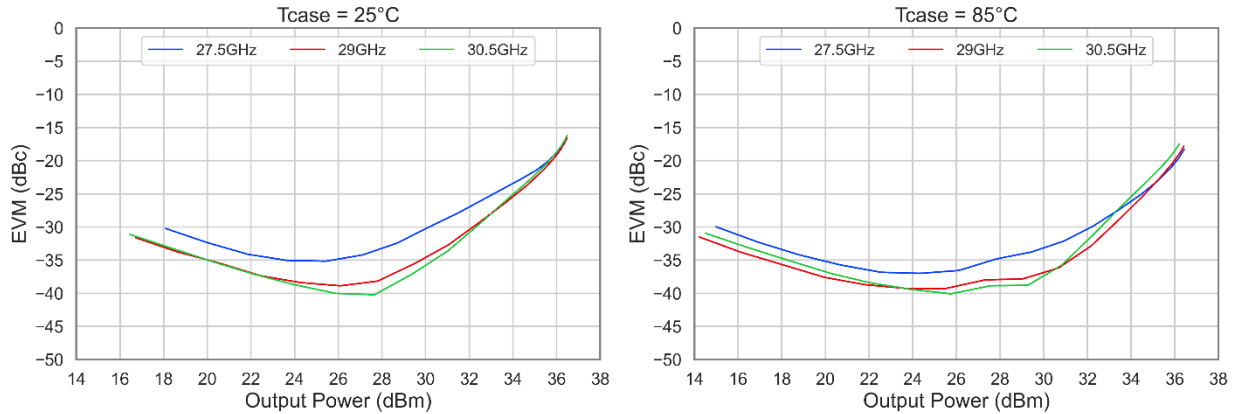


**Typical Board Measurements: Linearity – Modulated Signals**

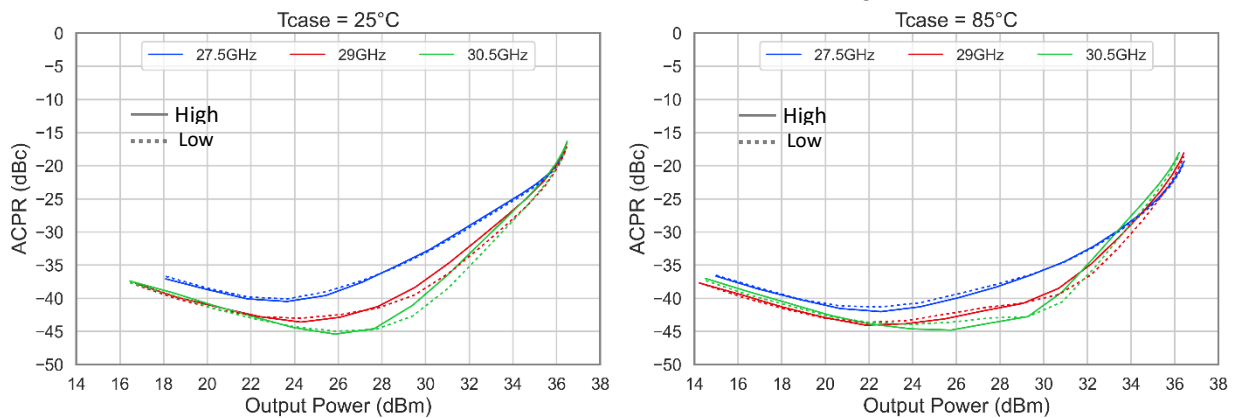
**Test conditions :** Modulated signal,  $V_d = +25V$ ,  $I_{dq} = 140mA$ ,  $T_{backside} = 25^\circ C / 85^\circ C$ , **8PSK**, **BW = 100 MHz**, Roll-off = 0.2, PAPR=5dB

Board losses are de-embedded. Measurements are given in the die access plans.

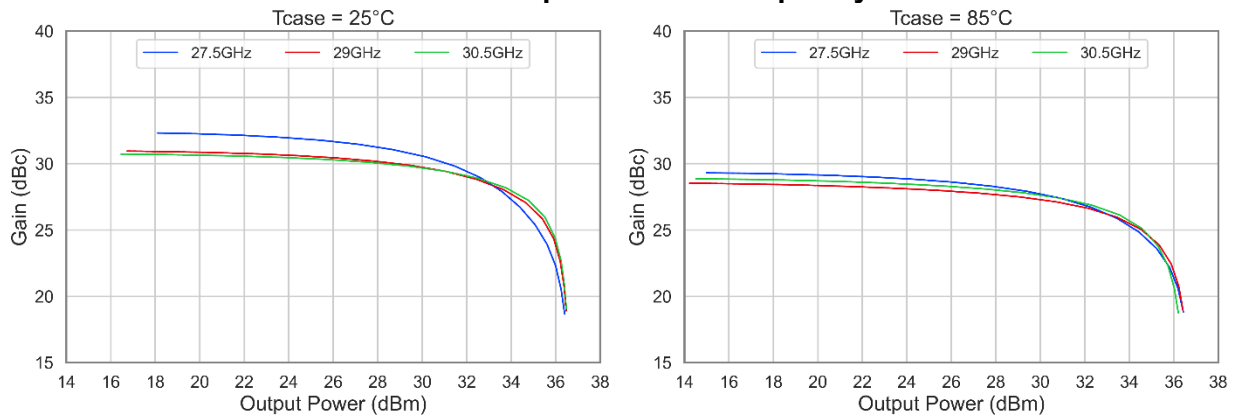
**EVM vs. Output Power & Frequency**



**ACPR vs. Output Power & Frequency**



**Gain vs. Output Power & Frequency**

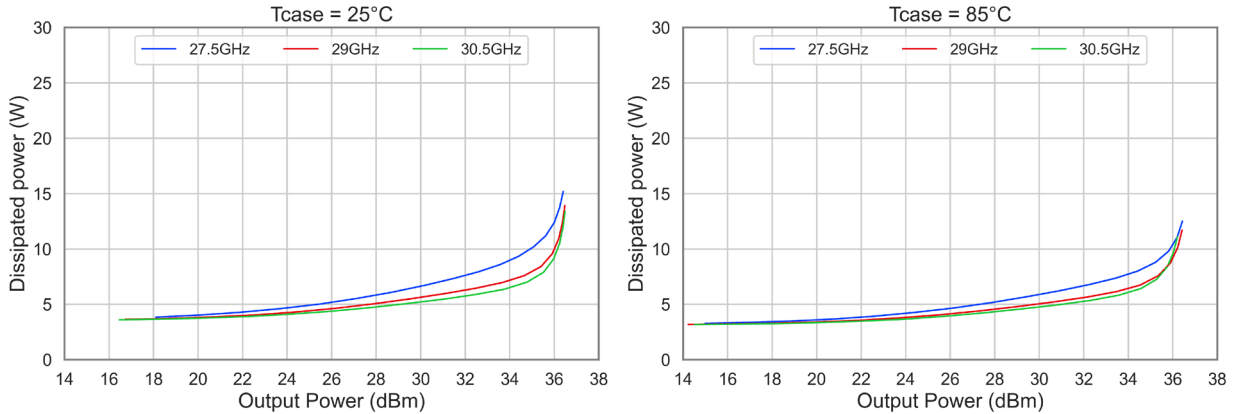


## Typical Board Measurements: Linearity – Modulated Signals

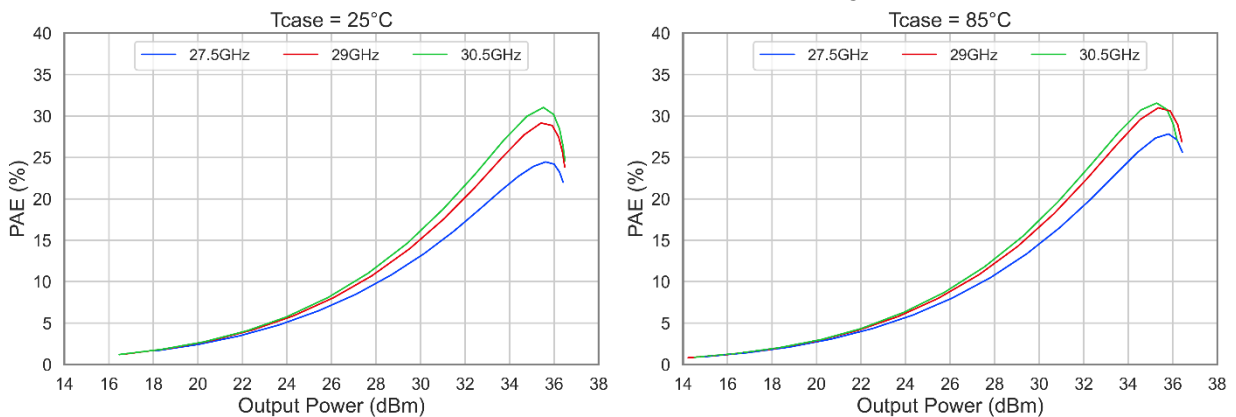
**Test conditions :** Modulated signal,  $V_d = +25V$ ,  $I_{dq} = 140mA$ ,  $T_{backside} = 25^{\circ}C / 85^{\circ}C$ , **8PSK**, **BW = 100 MHz**, Roll-off = 0.2, PAPR=5dB

Board losses are de-embedded. Measurements are given in the die access plans.

### Dissipated Power vs. Output Power & Frequency



### PAE vs. Output Power & Frequency

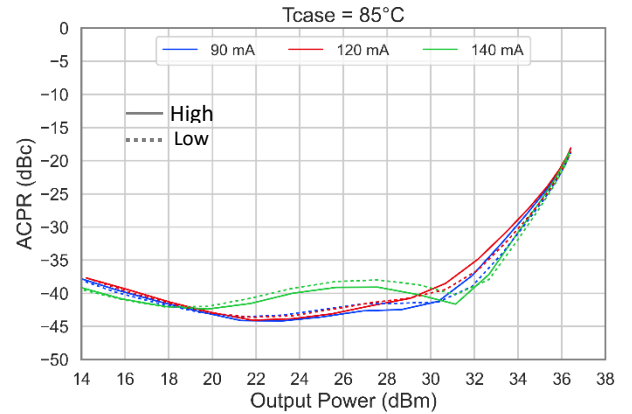
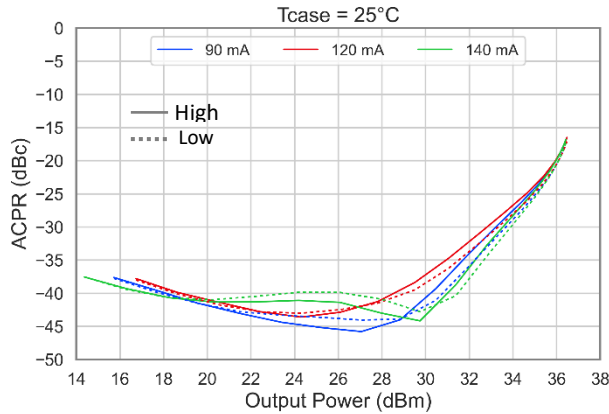


**Typical Board Measurements: Linearity – Modulated Signals**

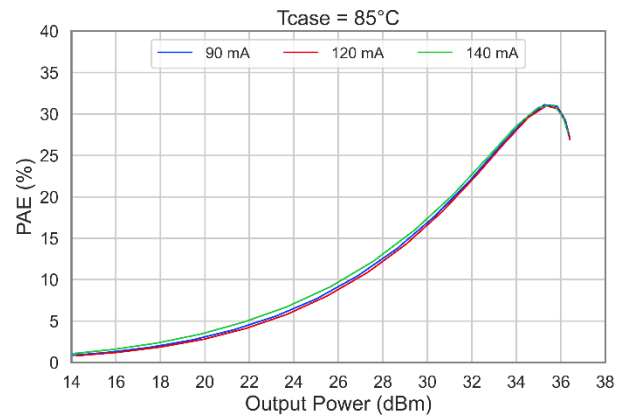
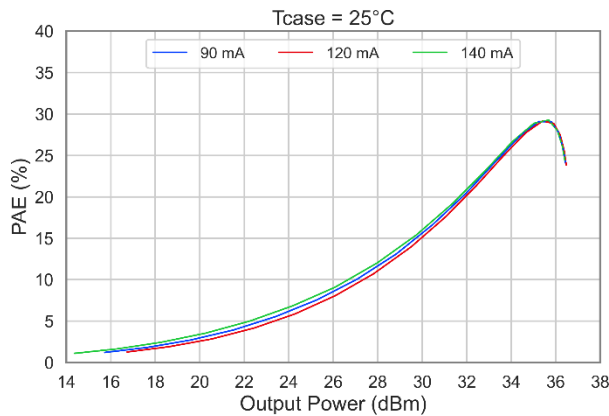
**Test conditions :** Modulated signal, Vd = +25V, Freq=29 GHz, T<sub>backside</sub> = 25°C / 85 °C , **8PSK**, **BW = 100 MHz**, Roll-off = 0.2, PAPR=5dB

Board losses are de-embedded. Measurements are given in the die access plans.

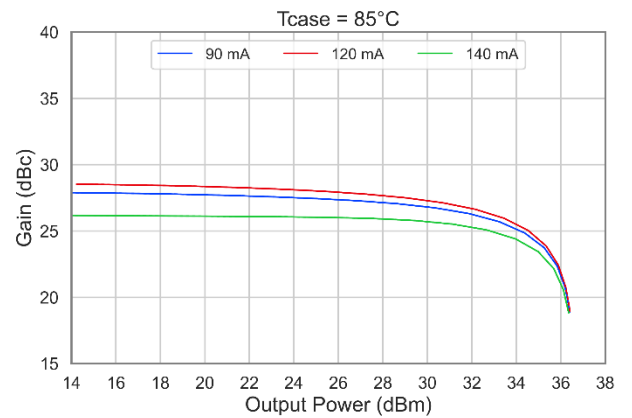
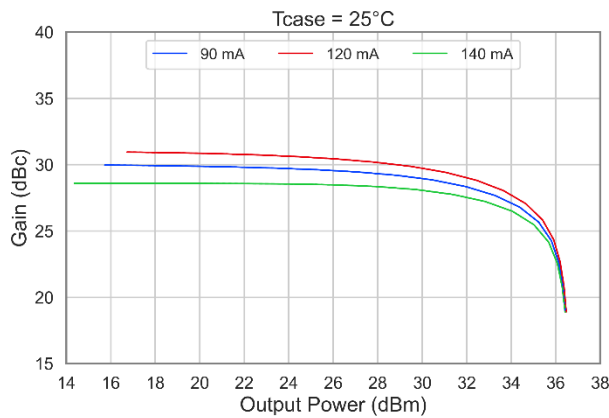
**ACPR vs. Output Power & Idq**



**PAE vs. Output Power & Idq**



**Gain vs. Output Power & Idq**

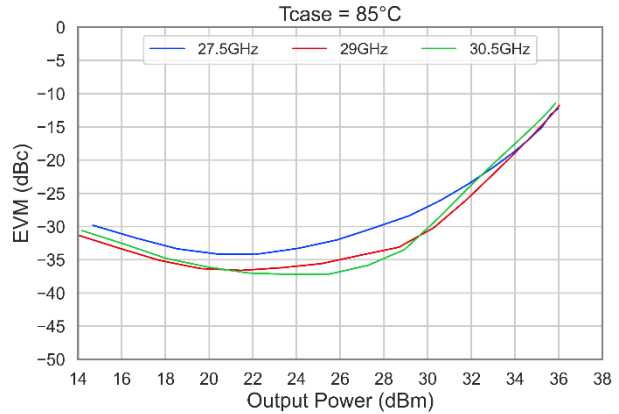
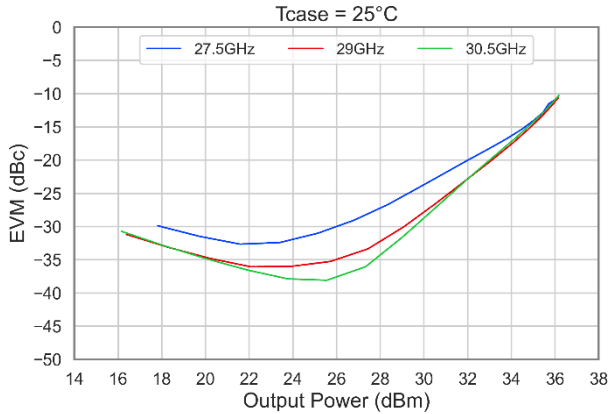


## Typical Board Measurements: Linearity – Modulated Signals

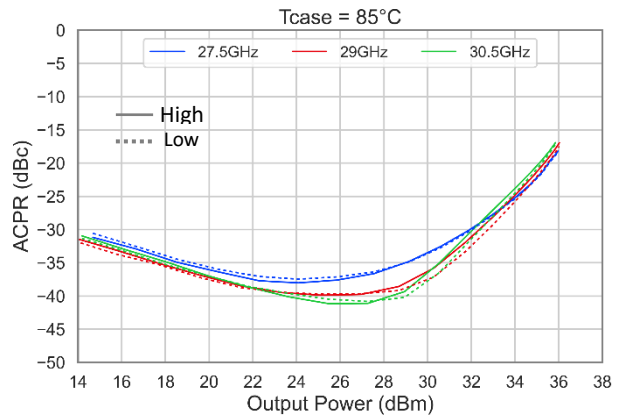
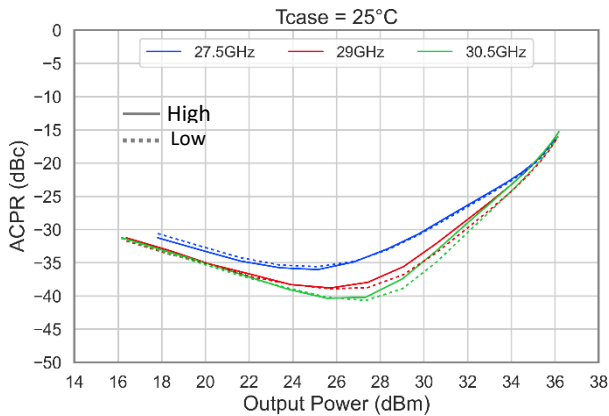
**Test conditions :** Modulated signal ,  $V_d = +25V$ ,  $I_{dq} = 140mA$ ,  $T_{backside} = 25^\circ C / 85^\circ C$  , **256QAM**, **BW = 100 MHz**, Roll-off = 0.2, PAPR=7.221dB

Board losses are de-embedded. Measurements are given in the die access plans.

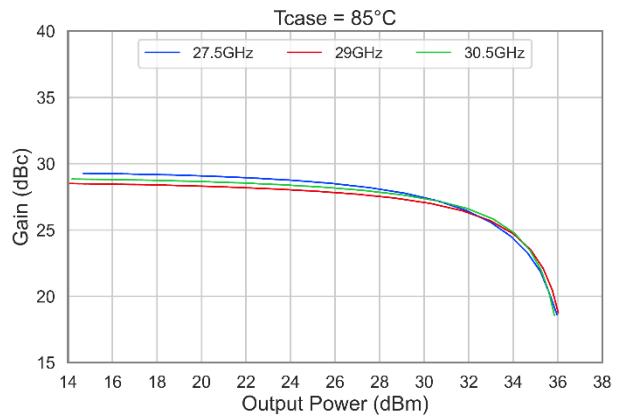
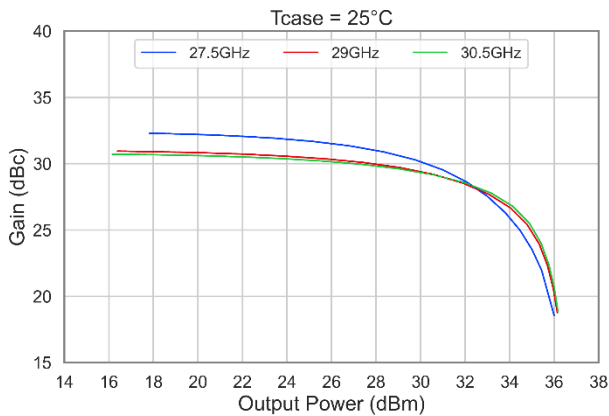
### EVM vs. Output Power & Frequency



### ACPR vs. Output Power & Frequency



### Gain vs. Output Power & Frequency

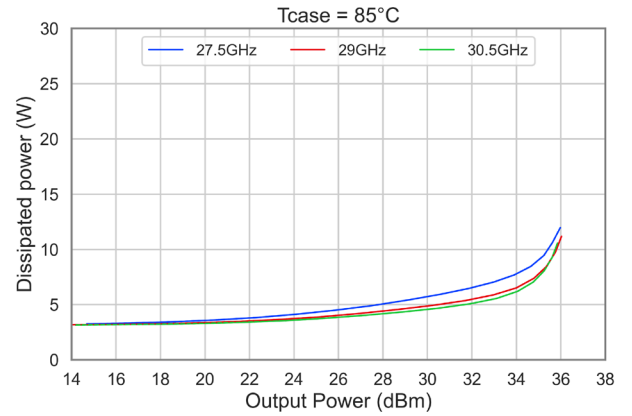
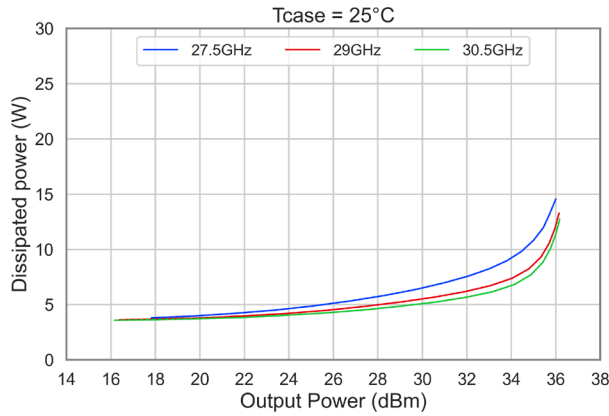


**Typical Board Measurements: Linearity – Modulated Signals**

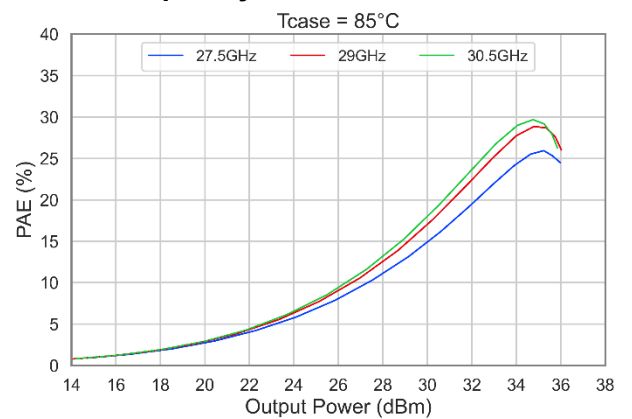
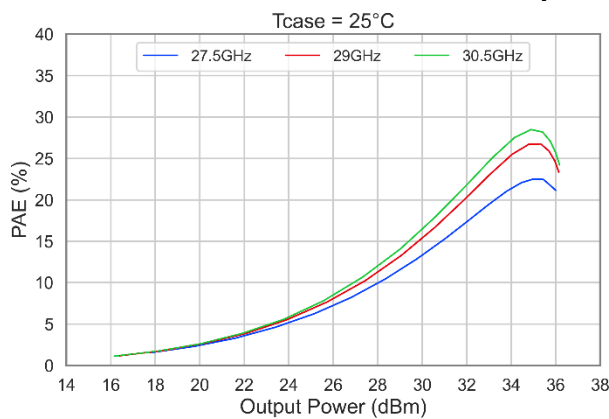
**Test conditions** :Modulated signal , Vd = +25V, Idq = 140mA, T<sub>backside</sub> = 25°C / 85 °C , **256QAM**, **BW = 100 MHz**, Roll-off = 0.2, PAPR=7.221dB

Board losses are de-embedded. Measurements are given in the die access plans.

**Dissipated Power vs. Output Power & Frequency**



**PAE vs. Output Power & Frequency**

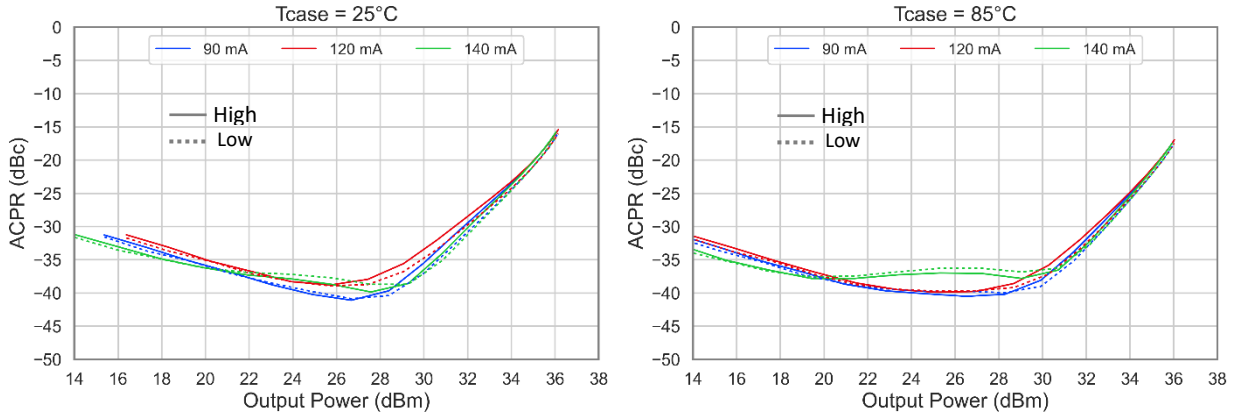


## Typical Board Measurements: Linearity – Modulated Signals

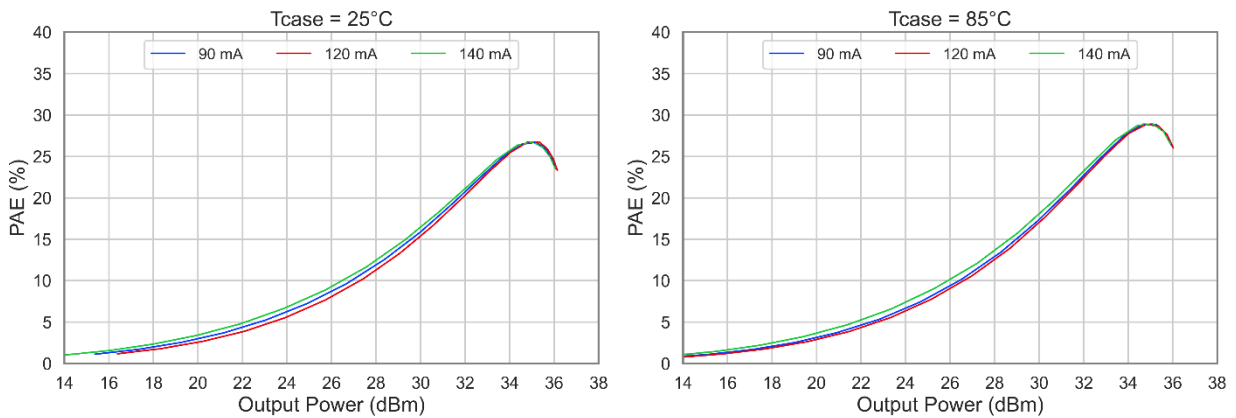
**Test conditions** : Modulated signal ,  $V_d = +25V$ ,  $Freq = 29\text{ GHz}$ ,  $T_{backside} = 25^\circ\text{C} / 85^\circ\text{C}$  , **256QAM**, **BW = 100 MHz**, Roll-off = 0.2, PAPR=7.221dB

Board losses are de-embedded. Measurements are given in the die access plans.

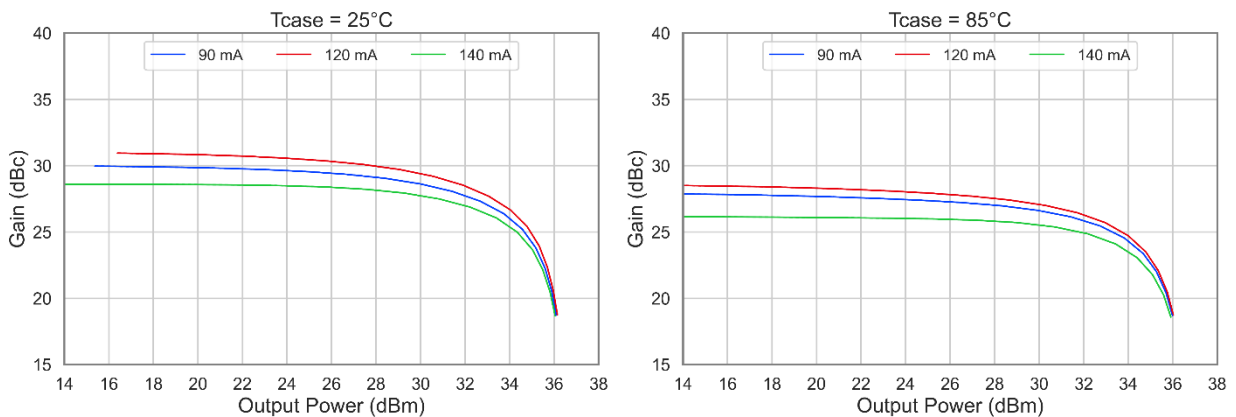
### ACPR vs. Output Power & Idq



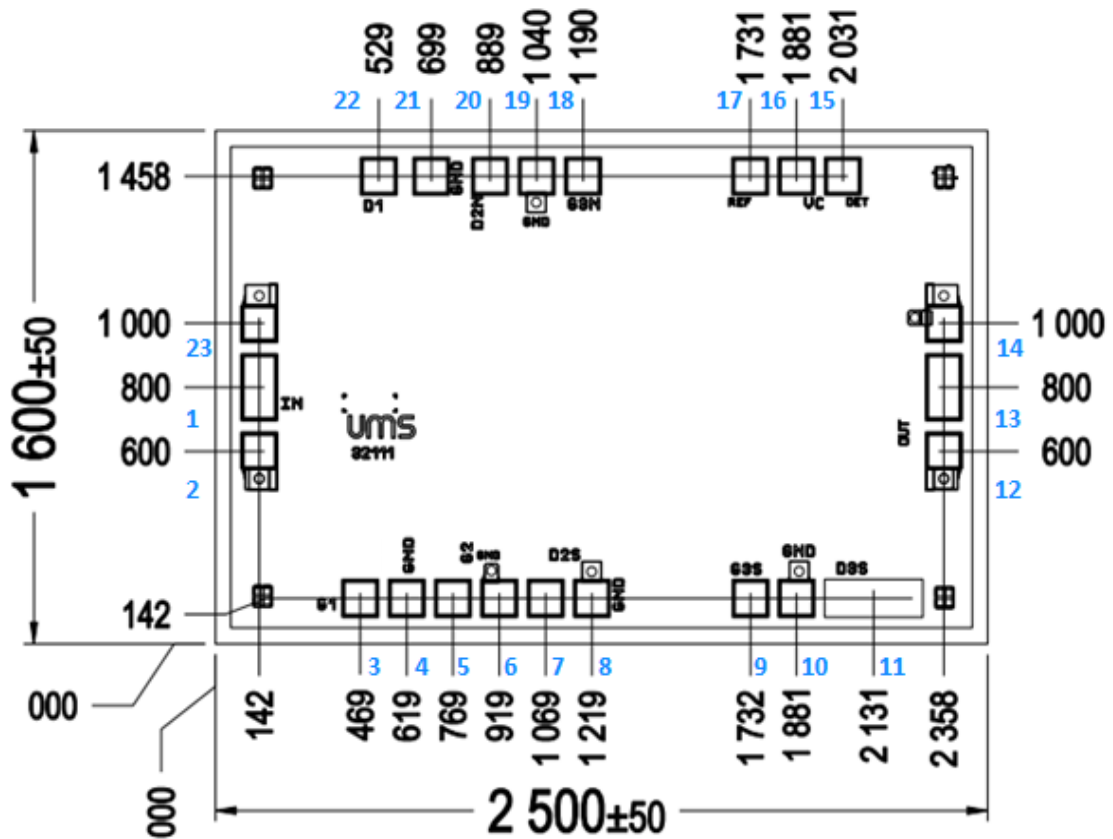
### PAE vs. Output Power & Idq



### Gain vs. Output Power & Idq

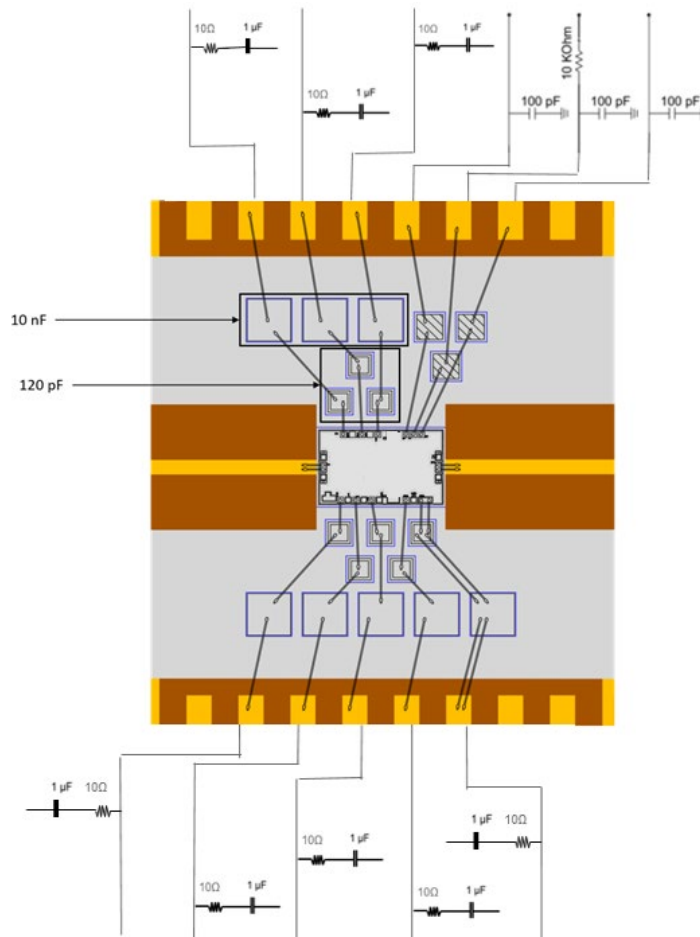
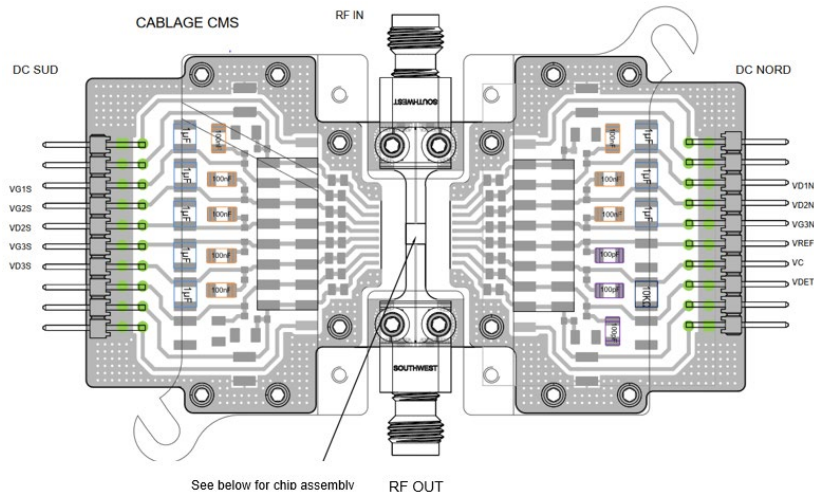


**Chip Mechanical Data**



Pin number	Pin name	Description
1	IN	Input RF port
2, 4, 6, 8, 10, 12, 14, 19, 21, 23	GND	Ground
3	G1	Negative supply voltage (gate of stage 1)
5	G2	Negative supply voltage (gate of stage 2)
7	D2S	Positive supply voltage (drain of south stage 2)
9	G3S	Negative supply voltage (gate of south stage 3)
11	D3S	Positive supply voltage (drain of south stage 3)
13	OUT	Output RF port
15	DET	Detector DET measurement Pin
16	VC	Detector positive supply (typical : 5V)
17	REF	Detector REF measurement Pin
18	G3N	Negative supply voltage (gate of north stage 3)
20	D2N	Positive supply voltage (drain of north stage 2)
22	D1	Positive supply voltage (drain of north stage 1)

## Evaluation Board (EVB)



3 levels of decoupling capacitors have been used: 2 on the tab and 1 on the board. The first level is composed of 120 pF chip capacitors. The second level is composed of 10nF chip capacitors. The third level is made with 1 $\mu$ F SMD 1206 capacitors (and 10 ohms added in series). The first two levels should be as close as possible to the die.

Note: All board measurements are performed using **shielded cables**, even for DC bias, to ensure safe operation.

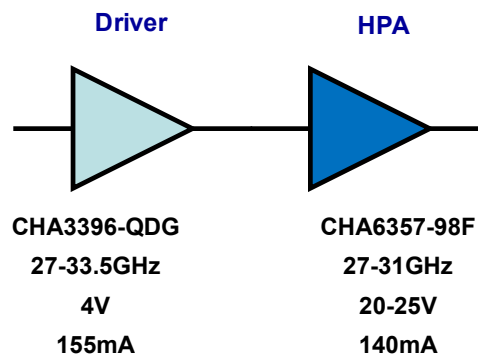
**ESD sensitivity**

Parameter	Classification	Standard
Human Body Model (HBM)	1A	ANSI/ESDA/JEDEC - JS-001

**Recommended UMS Power chain**

The CHA6357 is recommended with the CHA3396-QDG.

For more information about the CHA3396-QDG, see our web site [www.ums-rf.com](http://www.ums-rf.com)



## Recommended reflow process assembly

Refer to the application note AN0001 available at <https://www.ums-rf.com> for die attach.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

## Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS products.

## Recommended Evaluation board assembly

Refer to the application note AN0030 available at <https://www.ums-rf.com> Evaluation board.

## Ordering Information

Chip form	CHA6357-98F/00
Evaluation board	EVB-CHA6357-98F

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.**. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**