United Monolithic Semiconductors

CHP3010a98F

L-Band 6-Bit Digital Phase Shifter

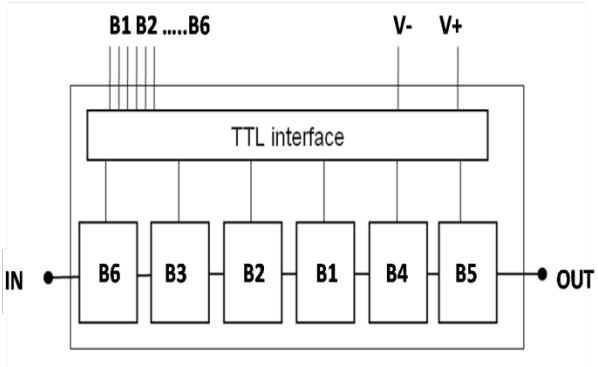
GaAs Monolithic Microwave IC

Description

CHP3010a98F is an L-Band (1.2 - 1.4GHz) monolithic 6-bit digital phase-shifter with a 0-360° range and a high phase accuracy. The typical RMS phase error is 1.5°. The circuit provides 7dB insertion loss associated with input and output return losses better than 15dB under all logic states. An on-chip DC-interface is compatible with both CMOS (0/+3.3V) and TTL (0/+5V) logics.

The circuit is mainly dedicated to radar systems and is also well suited for a wide range of microwave applications and systems.

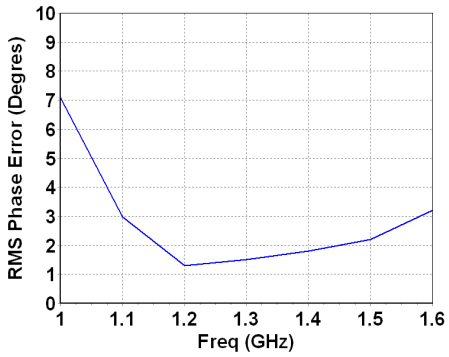
The MMIC is developed on a robust 0.25µm gate length pHEMT process and is also available packaged in a standard surface mount 32-lead QFN5x5.



Main Features

- 1.5 deg RMS Phase error
- Low I/O return losses (all states)
- 24dBm Input P-1dB
- 16dBm Output P-1dB
- CMOS /TTL compatibility: V+ = +3.3/5 Volt
- DC-decoupled I/O
- Chip size 3.37x2.73x0.1mm

RMS Phase Error vs. Frequency



Main Electrical Characteristics

Tbackside= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	1.2		1.4	GHz
PPE	Peak Phase Error		(-1,+3)		deg
RMS_PE	RMS Phase Error		1.5		deg
P1dB	Input power @ 1dBcomp (CW)		24		dBm

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Electrical Characteristics

Tbackside= +25°C

Symbol	Parameter	Min	Typ.	Max	Unit
Fop	Operating frequency range	1.2		1.4	GHz
PhS	Phase Shifting Range	0		360	deg
PhS step	Phase Shifting Step		5.625		deg
PPE	Peak Phase Error		(- 1, +3)		deg
RMS_PE	RMS Phase Error		1.5		deg
IL	Insertion Loss		7		dB
Av	Amplitude Variation		±0.5		dB
RMS_Av	RMS Amplitude Variation		0.15		dB
VSWR_In	Input Return Loss		15		dB
VSWR_Out	Output Return Loss		15		dB
P1dB	Input power @ 1dBcomp (CW)		24		dBm
OP1dB	Output power @ 1dBcomp (CW)		16		dBm
Tswitch	Switching Time		30		ns
Vlow	Control Input – low level	0		0.4	V
Vhigh	Control Input – high level	2.4		5	V
V+	Positive Supply Voltage		5 , 3.3		V
V-	Negative Supply Voltage		- 5		V
I+	Positive Supply Current		4		mA
I-	Negative Supply Current		3.5		mA
Top	Operating temperature	-40		+85	deg

These values are representative of the chip's typical performances with bonding wires of 0.32nH at the RF ports.

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Absolute Maximum Ratings (1)

Tbackside= +25°C

Symbol	Parameter	Values	Unit
V+	Maximum DC positive supply voltage	+6	V
V-	Maximum DC negative supply voltage	-6	V
Vlow	Minimum phase shifter control voltage	-2	V
Vhigh	Maximum phase shifter control voltage	+6	V
Tj	Maximum junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

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Definitions

Peak Phase Error (PPE) definition

PPE(i) = measured_Phase(S21)@state(i) - measured_Phase(S21)@state(0) - theoreticalPhaseValue@State(i)

Amplitude Variation (Av) definition

Av(i) = Measured_dB(S21)@state(i) - Measured_dB(S21)@state(0)

RMS Phase Error (RMS_PE) definition

$$RMS\_PE = \sqrt{\frac{\sum_{i=0}^{63} PPE^2(i)}{64}}$$

where i is the state number (from 0 to 63)

RMS Amplitude variation (RMS_Av) definition

$$RMS\_AV = \overline{Av} = \frac{\sum_{i=0}^{63} Av(i)}{64}$$

where i is the state number (from 0 to 63)

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Typical Bias Conditions

Two options are possible for the positive value of the biasing circuit without any impact on RF performances.

Option 1

Symbol	PAD N°	Parameter	Values	Unit
V+	4	Positive Supply Voltage	+5	V
V-	5	Negative Supply Voltage	-5	V
V+	6	Positive Supply Voltage	NC	
Bit1 to Bit6	7 to 12	Control Input Voltage	0 / +3.3	V

Option 2

Symbol	PAD N°	Parameter	Values	Unit
V+	4	Positive Supply Voltage	+3.3	V
V-	5	Negative Supply Voltage	-5	V
V+	6	Positive Supply Voltage	+3.3	V
Bit1 to Bit6	7 to 12	Control Input Voltage	0 / +3.3	V

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Device thermal information

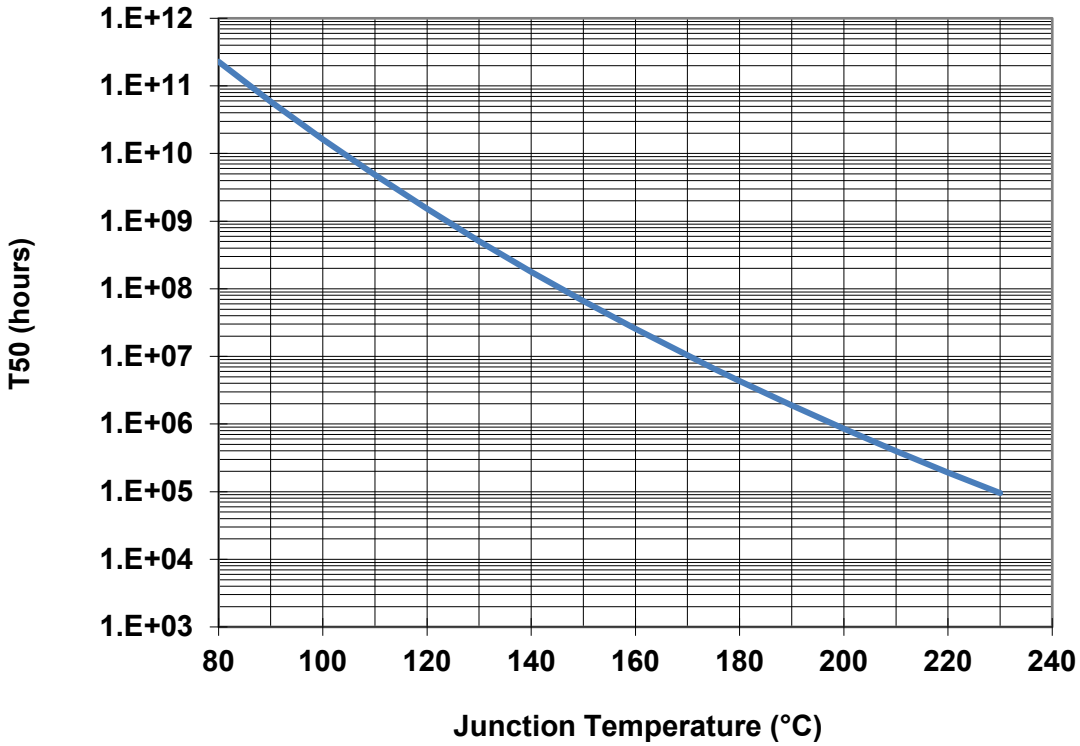
All the figures given in this section are obtained assuming that the die is only cooled down by conduction through the chip backside.
The temperature is monitored at the chip back-side interface (Tbackside).
For nominal operating, the system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Recommended Operating Ratings table.
So, the system PCB must be designed to comply with this requirement.

Thermal Resistance(1)	Rth_eq	$T_{backside}$ =85°C, V+=+3.3V, V-=-5V, I+=4mA	1	°C/W
Junction Temperature	Tj		85	°C
Median Life	T50		> $9.0x10^{10}$	Hrs

At input P1dB (Pin=24 dBm) expect Rth_eq in the range of 7.5°C/W, Tj still remains in the range of 85°C.

(1) The Rth_equivalent is extrapolated, taking into account the full DC power and the channel temperature increase on the hottest transistor.

Median Life Time vs. Junction Temperature



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Phase shifter control table

Voltage to apply on Bit 1 to Bit 6 (pads 7 to 12):

State	Phase (deg)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	State	Phase (deg)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
0	0	0	0	0	0	0	0	32	180	3.3	0	0	0	0	0
1	5.625	0	0	0	0	0	3.3	33	185.625	3.3	0	0	0	0	3.3
2	11.25	0	0	0	0	3.3	0	34	191.25	3.3	0	0	0	3.3	0
3	16.875	0	0	0	0	3.3	3.3	35	196.875	3.3	0	0	0	3.3	3.3
4	22.5	0	0	0	3.3	0	0	36	202.5	3.3	0	0	3.3	0	0
5	28.125	0	0	0	3.3	0	3.3	37	208.125	3.3	0	0	3.3	0	3.3
6	33.75	0	0	0	3.3	3.3	0	38	213.75	3.3	0	0	3.3	3.3	0
7	39.375	0	0	0	3.3	3.3	3.3	39	219.375	3.3	0	0	3.3	3.3	3.3
8	45	0	0	3.3	0	0	0	40	225	3.3	0	3.3	0	0	0
9	50.625	0	0	3.3	0	0	3.3	41	230.625	3.3	0	3.3	0	0	3.3
10	56.25	0	0	3.3	0	3.3	0	42	236.25	3.3	0	3.3	0	3.3	0
11	61.875	0	0	3.3	0	3.3	3.3	43	241.875	3.3	0	3.3	0	3.3	3.3
12	67.5	0	0	3.3	3.3	0	0	44	247.5	3.3	0	3.3	3.3	0	0
13	73.125	0	0	3.3	3.3	0	3.3	45	253.125	3.3	0	3.3	3.3	0	3.3
14	78.75	0	0	3.3	3.3	3.3	0	46	258.75	3.3	0	3.3	3.3	3.3	0
15	84.375	0	0	3.3	3.3	3.3	3.3	47	264.375	3.3	0	3.3	3.3	3.3	3.3
16	90	0	3.3	0	0	0	0	48	270	3.3	3.3	0	0	0	0
17	95.625	0	3.3	0	0	0	3.3	49	275.625	3.3	3.3	0	0	0	3.3
18	101.25	0	3.3	0	0	3.3	0	50	281.25	3.3	3.3	0	0	3.3	0
19	106.875	0	3.3	0	0	3.3	3.3	51	286.875	3.3	3.3	0	0	3.3	3.3
20	112.5	0	3.3	0	3.3	0	0	52	292.5	3.3	3.3	0	3.3	0	0
21	118.125	0	3.3	0	3.3	0	3.3	53	298.125	3.3	3.3	0	3.3	0	3.3
22	123.75	0	3.3	0	3.3	3.3	0	54	303.75	3.3	3.3	0	3.3	3.3	0
23	129.375	0	3.3	0	3.3	3.3	3.3	55	309.375	3.3	3.3	0	3.3	3.3	3.3
24	135	0	3.3	3.3	0	0	0	56	315	3.3	3.3	3.3	0	0	0
25	140.625	0	3.3	3.3	0	0	3.3	57	320.625	3.3	3.3	3.3	0	0	3.3
26	146.25	0	3.3	3.3	0	3.3	0	58	326.25	3.3	3.3	3.3	0	3.3	0
27	151.875	0	3.3	3.3	0	3.3	3.3	59	331.875	3.3	3.3	3.3	0	3.3	3.3
28	157.5	0	3.3	3.3	3.3	0	0	60	337.5	3.3	3.3	3.3	3.3	0	0
29	163.125	0	3.3	3.3	3.3	0	3.3	61	343.125	3.3	3.3	3.3	3.3	0	3.3
30	168.75	0	3.3	3.3	3.3	3.3	0	62	348.75	3.3	3.3	3.3	3.3	3.3	0
31	174.375	0	3.3	3.3	3.3	3.3	3.3	63	354.375	3.3	3.3	3.3	3.3	3.3	3.3

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Typical on-wafer Sij parameters (state 0)

Tbackside= +25°C, V+ = +5V, V- = -5V

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
0.5	-5.645	-43.58	-23.25	95.52	-23.09	95.4	-2.881	101.1
0.6	-7.538	-84.12	-17.48	61.46	-17.46	61.36	-3.228	82.98
0.7	-12.08	-135.7	-13.04	21.37	-13.06	21.25	-4.13	62.46
0.8	-18.65	133.9	-10.06	-20.85	-10.06	-21.12	-5.835	41.73
0.9	-17.58	38.43	-8.231	-62.63	-8.224	-62.7	-8.345	21.9
1	-16.95	-8.87	-7.231	-101.8	-7.224	-101.8	-11.72	4.434
1.1	-19.31	-36.91	-6.762	-138	-6.752	-137.9	-16.32	-7.684
1.2	**-23.54**	**-37.77**	**-6.576**	**-171.8**	**-6.566**	**-171.8**	**-22.56**	**-13**
1.3	**-26.14**	**-21.16**	**-6.547**	**156.2**	**-6.536**	**156.1**	**-28.96**	**-1.011**
1.4	**-26.17**	**-11.96**	**-6.589**	**125.6**	**-6.583**	**125.5**	**-39**	**-35.27**
1.5	-27.31	6.5	-6.69	95.57	-6.686	95.51	-30.63	-145.9
1.6	-24.66	17.68	-6.902	66.11	-6.899	66.06	-22.15	-165.8
1.7	-21.56	12.64	-7.133	36.98	-7.125	36.86	-17.66	-177.3
1.8	-20.19	-11.38	-7.435	7.632	-7.421	7.488	-14.73	172
1.9	-20.24	-41.02	-7.82	-21.85	-7.809	-21.97	-12.81	164.4
2	-21.48	-82.73	-8.286	-52.44	-8.279	-52.58	-11.49	158.3
2.1	-26.13	-122.6	-9.131	-85.02	-9.125	-85.13	-10.17	157.7
2.2	-30.67	-80.41	-11.09	-118	-11.09	-118	-7.935	156.9
2.3	-19.26	-118.1	-13.87	-134.9	-13.88	-134.8	-5.551	145.7
2.4	-18.44	-173.2	-13.5	-150.2	-13.48	-150.2	-4.761	133.3
2.5	-22.71	166.5	-13.33	-179	-13.3	-179	-4.288	126.1
2.6	-21.62	-155	-14.2	150.1	-14.17	150.1	-3.736	120.3
2.7	-14.78	-158.3	-15.59	121.8	-15.6	121.6	-3.081	113.9
2.8	-10.96	-178.4	-17.25	96.26	-17.23	96.09	-2.625	107.5
2.9	-8.662	163.2	-18.82	73.22	-18.79	73.22	-2.272	101
3	-7.252	146.3	-20.07	51.84	-20.05	52.16	-2.035	95.29
3.1	-6.279	132.1	-20.96	31.25	-20.94	31.09	-1.923	89.64
3.2	-5.868	118.7	-21.49	9.244	-21.39	8.811	-1.829	84.97
3.3	-5.794	107.5	-21.67	-16.48	-21.57	-16.62	-1.883	80.74
3.4	-6.342	98.24	-21.75	-47.54	-21.76	-47.59	-1.873	77.53
3.5	-6.71	94.38	-22.63	-83.8	-22.67	-84.13	-1.849	75.38
3.6	-6.635	90.67	-24.83	-121.1	-24.77	-121	-1.595	73.01
3.7	-6.554	83.45	-27.64	-154.4	-27.6	-153.1	-1.379	70.04
3.8	-7.306	76.84	-30.61	177.6	-30.58	178.3	-1.235	66.43
3.9	-8.612	74.16	-33.86	151.8	-33.55	151.2	-1.123	63.3
4	-9.928	83.38	-37.39	124.8	-36.92	124.9	-1.105	59.97
4.1	-9.29	96.38	-40.7	100.9	-40.63	102.1	-1.04	57.08
4.2	-7.358	102.3	-43.97	89.09	-44.49	87.91	-1.141	53.98
4.3	-5.781	100.2	-48.06	82.7	-47.55	79.02	-1.257	51.45
4.4	-4.481	95.92	-50.06	71.71	-48.64	67.14	-1.421	50.59
4.5	-3.745	90.8	-51.07	39.48	-50.06	43.64	-1.238	49.64
5	-1.981	68.48	-55.75	-26.65	-59.84	-35.08	-0.8895	38.96
5.5	-1.279	53.69	-62.26	-92.52	-67.46	-159.6	-1.113	30.14
6	-0.958	42.24	-66.71	-11.88	-70.45	-177.6	-1.778	25.56

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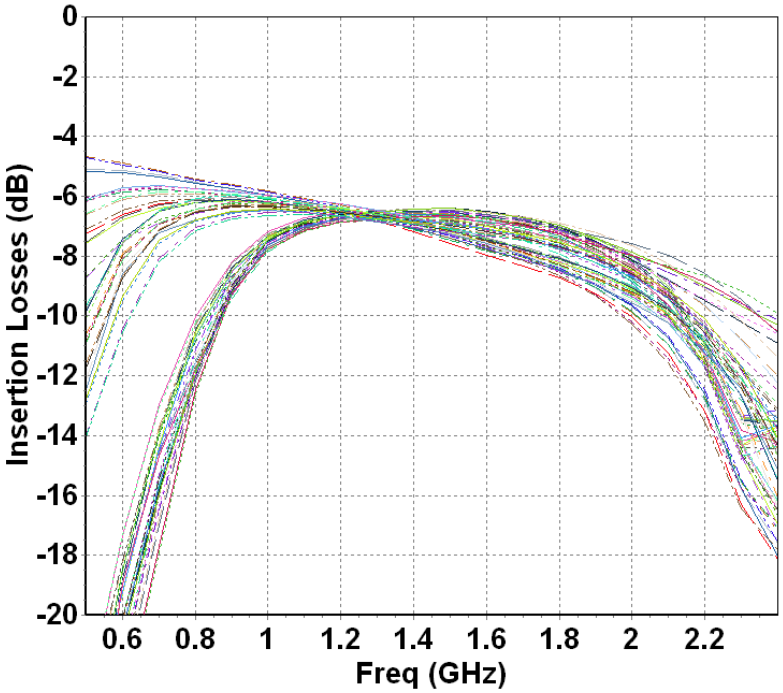
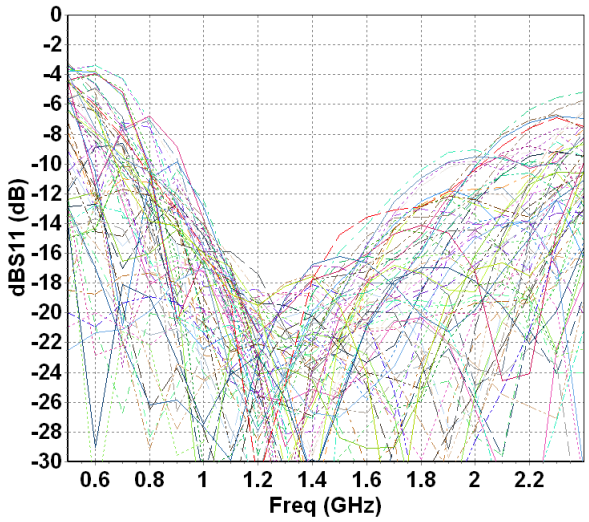
Typical on wafer Measurements

Tbackside= +25°C, V+ = +5V, V- = -5V

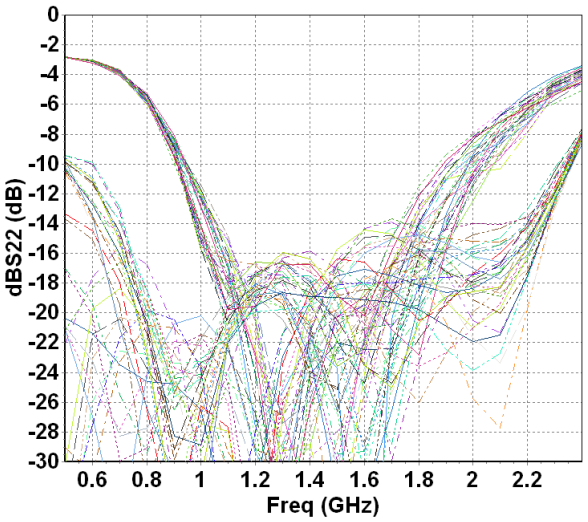
Insertion Losses vs. Frequency @ All States



Input Return Losses @ All States



Output Return Losses @ All States



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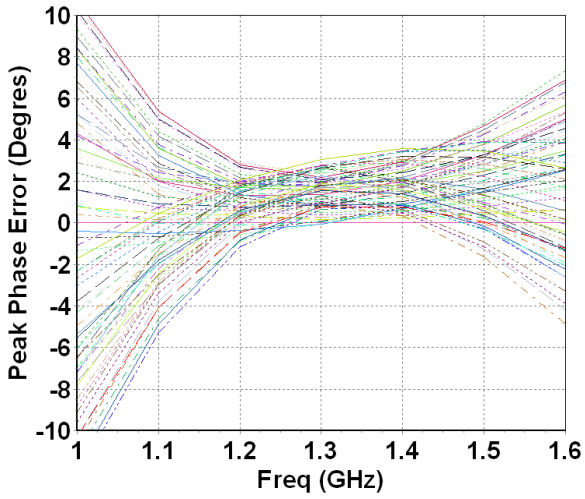
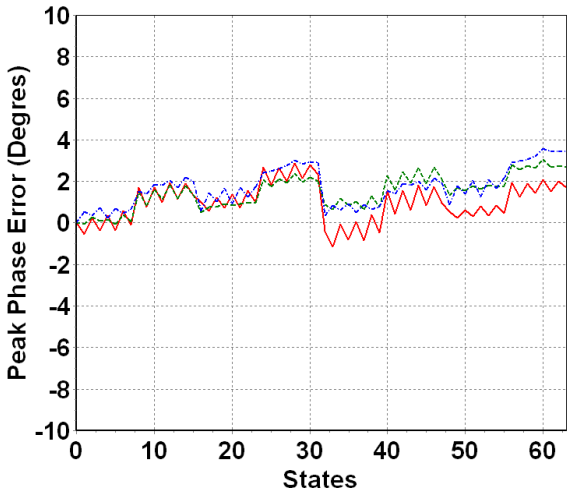
Peak Phase Error vs. Frequency (All States)

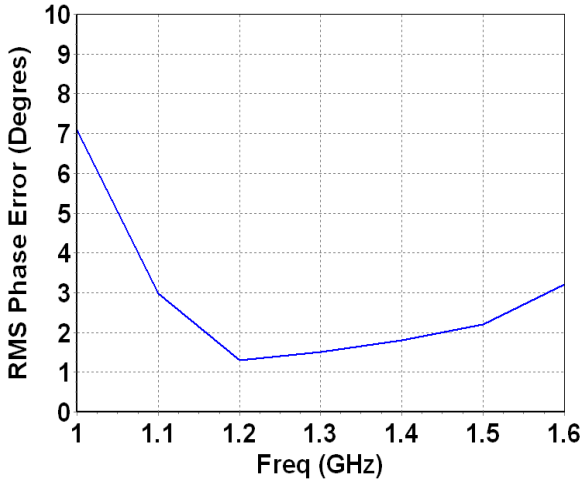


Peak Phase Error vs. States

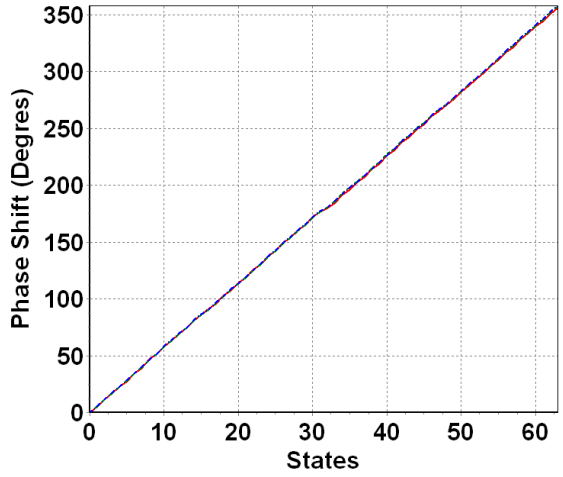


— 1.2GHz - - 1.3GHz — - 1.4GHz

RMS Phase Error vs. Frequency



Phase Shift vs. States (1.2 GHz ≤ Frequency ≤ 1.4GHz)



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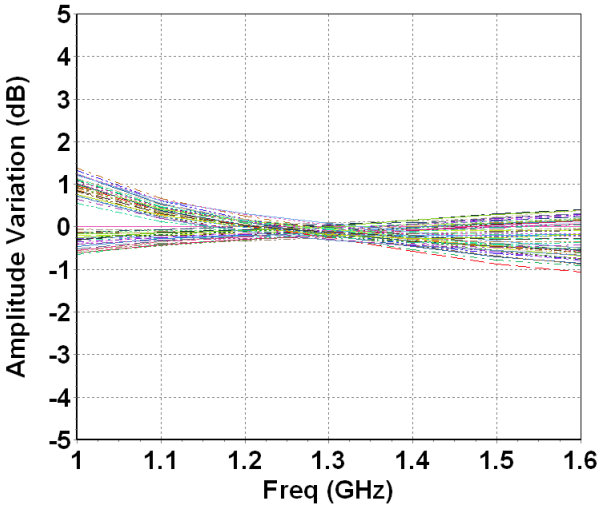
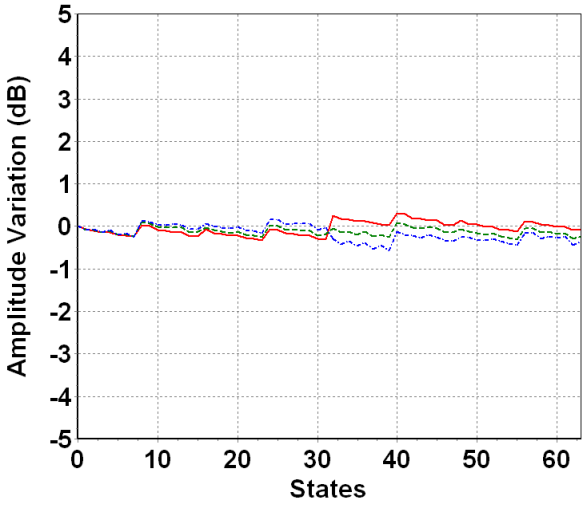
Amplitude Variation vs. Frequency (All States)

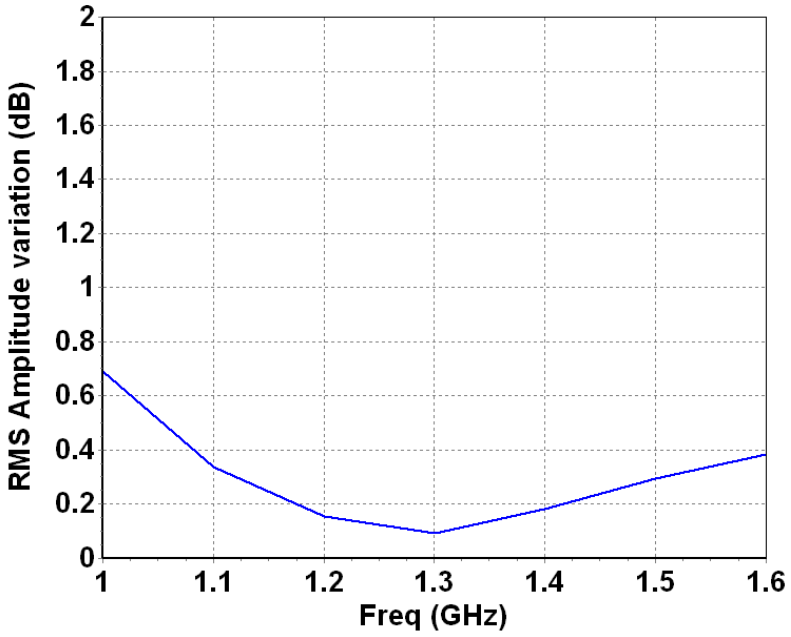


Amplitude Variation vs. States



— 1.2GHz - - 1.3GHz — - 1.4GHz

RMS Amplitude Variation vs. Frequency



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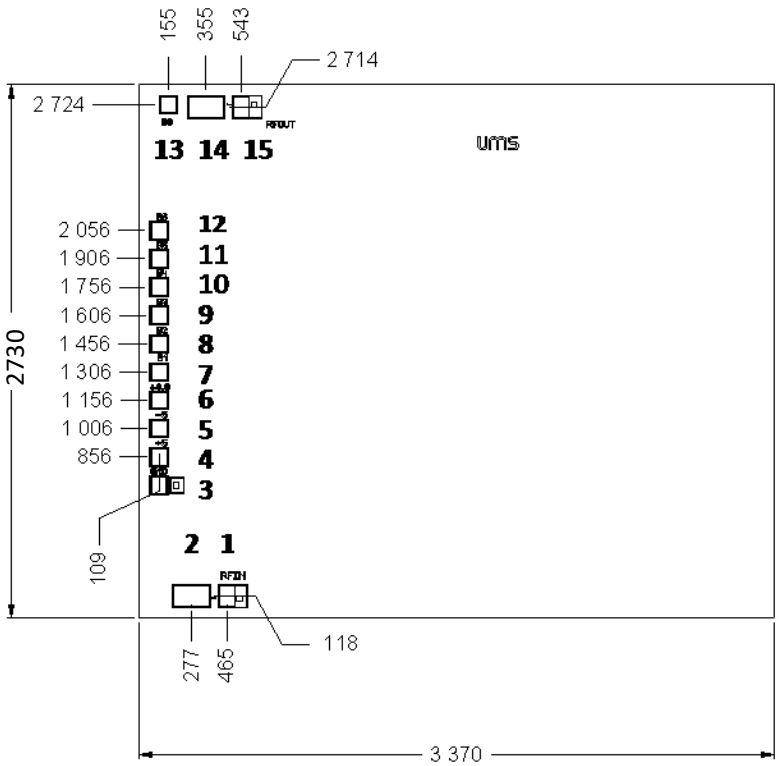
Mechanical dimensions and pad allocation



Unit : µm
Tolerance = ± 35µm

Pad number	Pad name	Description
1, 3, 15		Ground
2	RFIN	RF input
4	+5	+5V interface supply voltage (V+)
5	-5	-5V interface supply voltage (V-)
6	+3.3	+3.3V interface supply voltage (V+)
7	B1	Bit 1
8	B2	Bit 2
9	B3	Bit 3
10	B4	Bit 4
11	B5	Bit 5
12, 13	B6	Bit 6
14	RFOUT	RF output

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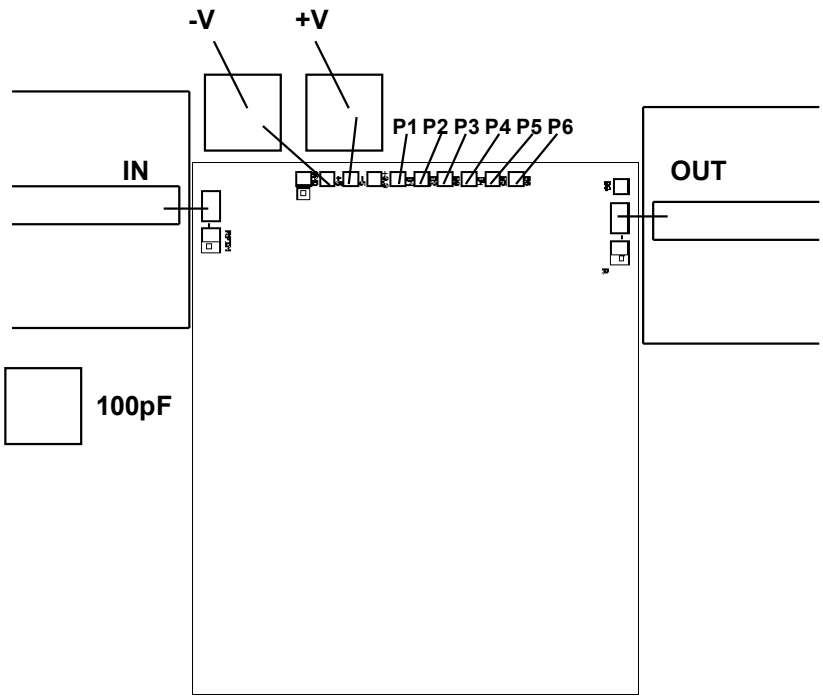
Recommended assembly plan



25µm wedge bonding is preferred

Bonding recommendations

Port	Connection
IN (2) OUT (14)	Inductance (Lbonding) = 0.32nH one wire: diameter 25µm, length 0.4mm
DC and Interface pads	Inductance (Lbonding) = 0.80nH one wire: diameter 25µm, length 1.0mm

Note:

An external capacitance is requested to protect the device from any external DC voltage that might be present on the RF accesses.

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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Ordering Information

Chip form:	CHP3010a98F/00

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