United Monolithic Semiconductors

CHA7063-QCB

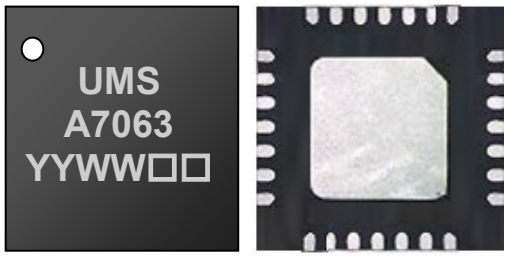
12.7-20GHz 5W Power Amplifier

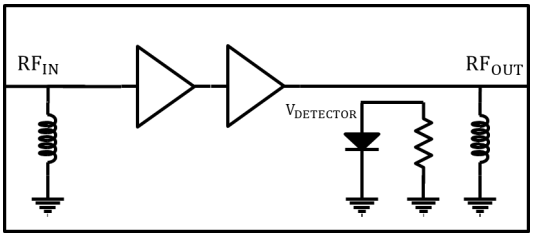
GaN Monolithic Microwave IC in SMD leadless package

Description

The CHA7063-QCB is a GaN monolithic Power Amplifier operating over 12.7-20GHz providing typically 5W saturated output power with 17% Power Added Efficiency. This amplifier exhibits 30dBm linear power with -33dBc ACPR at 200MHz 256QAM-OFDM and provides 20dB linear gain under 20V/216mA DC bias. It is dedicated to a wide range of applications such as Point-to-Point Radio, VSAT and Radar.

This circuit is manufactured on a robust GaN-on-SiC HEMT technology and packaged in a standard surface mount 5x5 plastic QFN which is RoHS compliant. Input and output are 50Ω matched and integrate ESD RF protections.



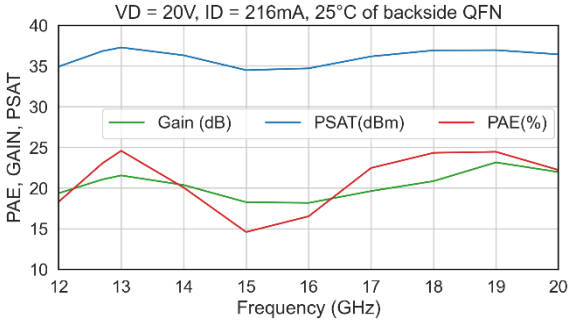


Main Features

- Frequency range: 12.7-20GHz
- Linear Gain: 20dB
- Psat: 37dBm
- ACPR < -33dBc at 30dBm Average Pout(1)
- EVM < 3% at 30dBm Average Pout(1)
- Output RF Power Detector
- DC bias: Vd = 20V @Idq = 216mA
- 28 leads QFN plastic package 5x5mm²
- MSL3

(1) 200MHz modulation bandwidth 256QAM-OFDM

Small Signal Gain, Output Power and PAE at Pin=25dBm, Tcase=25°C vs. Frequency



Main Electrical Characteristics

Tcase = 25°C (Tcase: QFN backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	12.7		20	GHz
Gain	Linear Gain		20		dB
ACPR	Adjacent Channel Power Ratio P_{out} = 30dBm 1024QAM BW=56MHz P_{out} = 30dBm 256QAM/OFDM BW=200MHz		 -35 -33		 dBc dBc
P_{sat}	Saturated output power		37		dBm

BW = modulation bandwidth

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Specifications

Tcase = 25°C, Vd = 20V (QFN reference plans)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	12.7		20	GHz
Gain	Linear Gain		20		dB
ΔG	Gain variation in temperature		± 0.03		dB/ °C
ΔVg /ΔG	Gain Control		10		mV/ dB
S11(1)	Input Return Loss		14		dB
S22(1)	Output Return Loss		9		dB
Psat	Saturated output power		37		dBm
PAE	Power Added Efficiency at Psat		17		%
ACPR	ACPR @ P_{AVG}=30dBm, 256QAM 200MHz modulation bandwidth		-35		dBc
EVM	EVM @ P_{AVG}=30dBm for 256QAM, 200MHz modulation bandwidth		-32		dB
IMD3	Third Order Intermodulation Distortion P_{out} = +31dBm / Tone		-25		dBc
Pdc @ 29dBm	DC power consumption @ 29dBm Output power		8		W
Dr	Detection dynamic range (for output power detection up to Psat)		30		dB
Vdetect	Voltage detection V_{REF} - V_{DET} up to Psat		10 to 2200		mV
Vg	DC Gate voltage		-2.85		V
Id	Total Drain bias current		216		mA

These values are representative of measurements performed on evaluation board as defined on the drawing in paragraph "Evaluation board".

(1) Input and Output Return Loss are given at RF reference plan of the Evaluation board (see Definition of the Sij reference plans section).

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Absolute Maximum Ratings (1)

Tcase = 25°C

Symbol	Parameter	Value	Unit
Vd	Drain bias voltage	27	V
Vg	Gate bias voltage range	-7 to -2	V
Idq	Quiescent Drain bias current	320	mA
Pin	Maximum input power	+27	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range (3), (4)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	20	V
Vg	Gate bias voltage	-5 to -2.7	V
Idq	Quiescent Drain bias current	216	mA
Pin	Maximum Input power	+25	dBm
Tj	Maximum Junction temperature (2)	200	°C

(2) See Device thermal performances section
(3) Electrical performances are defined for specified test conditions
(4) Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

Tcase	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tcase = 25°C

Symbol	Pin Nº	Parameter	Values	Unit
Vd	9, 13, 23, 27	Drain voltage	20	V
Vg	8, 11, 25, 28	Gate voltage	-3	V
Id		DC Drain bias current	216	mA
Vc	21	Detector voltage supply	5	V

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“Power ON” sequence

1. Bias HPA gate voltage at Vg (VG1N/S, VG2N/S) close to Vpinch-off (Vg ≈ -5V)
2. Set Vd (VD1N/S, VD2N/S) bias voltage to 0V: Id = 0mA
3. Apply Vd (VD1N/S, VD2N/S) bias voltage, Vd = 20V: Id = 0mA
4. Set Vc bias voltage to 5V for Detector biasing
5. Increase Vg (VG1N/S, VG2N/S) up to quiescent bias drain current Idq
6. Apply RF input Power

“Power OFF” sequence

1. Turn off RF input power
2. Bias HPA Gate voltage at Vg (VG1N/S, VG2N/S) ≈ -5V: Id = 0mA
3. Decrease Vd (VD1N/S, VD2N/S) bias voltage down to 0V
4. Set Vc bias voltage to 0V
5. Turn Vg (VG1N/S, VG2N/S) bias voltage to 0V

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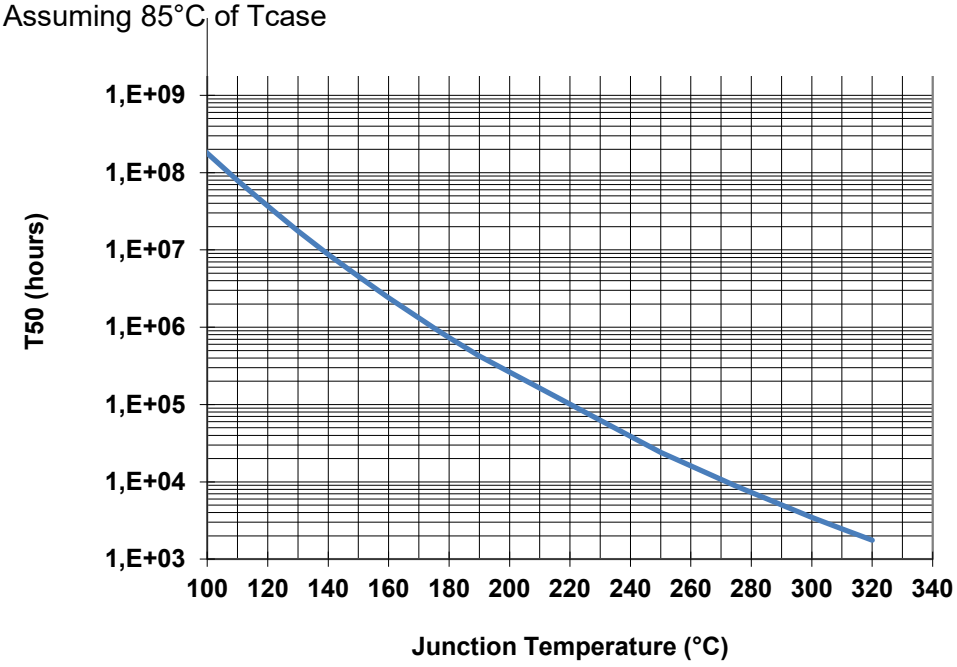
Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase).
For nominal operating, the system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Recommended Operating Ratings table.
Therefore, the system PCB must be designed to comply with this requirement.

Thermal Resistance (1)	R_{TH}	Tcase = 85°C, Vd = 20V, Idq = 216 mA, CW Pout = 32 dBm, Pdiss = 8.66 W	8.55	°C/W
Junction Temperature	Tj		159	°C
Median Life	T50		2.5E+6	hours
Thermal Resistance (1)	R_{TH}	Tcase = 85°C, Vd = 20V, Idq = 216 mA, CW Pout = 37 dBm, Pdiss = 15 W	7.14	°C/W
Junction Temperature	Tj		192	°C
Median Life	T50		3.0E+05	hours

(1) Assuming 85°C of Tcase



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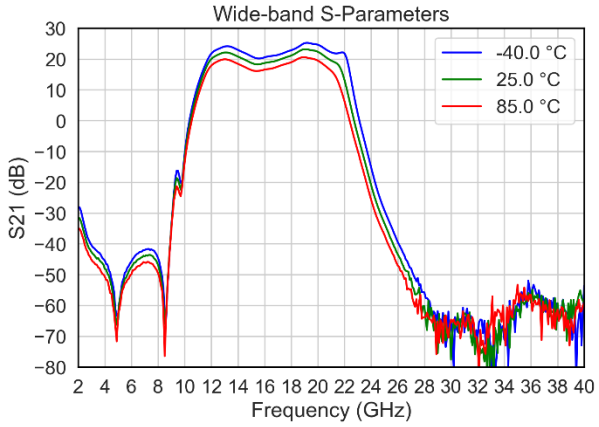
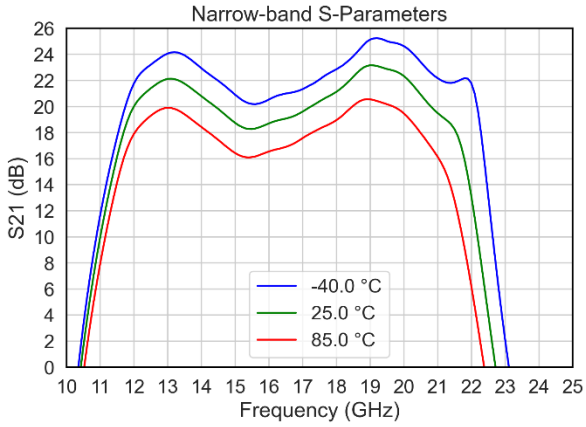
Typical Board Measurements: Small Signal Performances

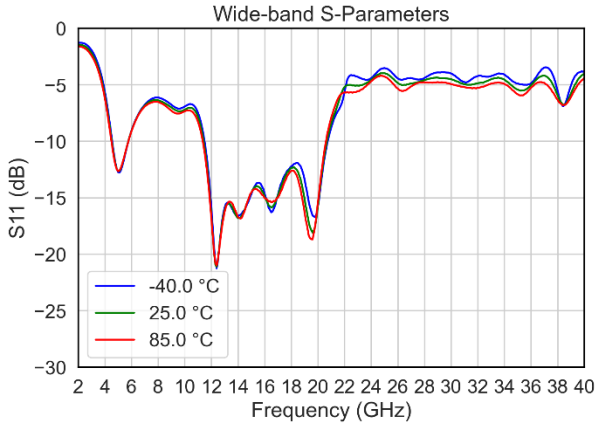
Performance vs. temperature

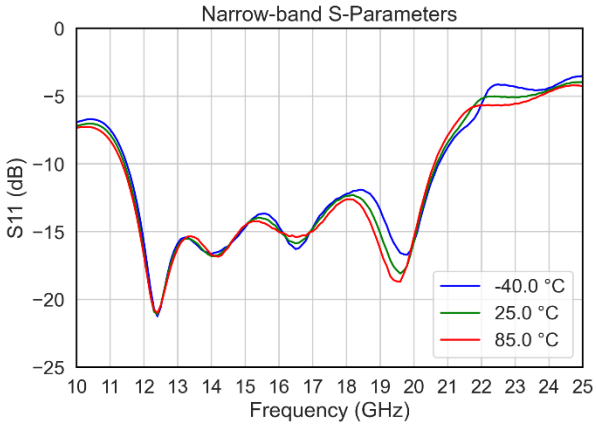
Test conditions: CW, Vd = 20V, Idq = 216mA, Tcase = -40°C / 25°C / 85 °C

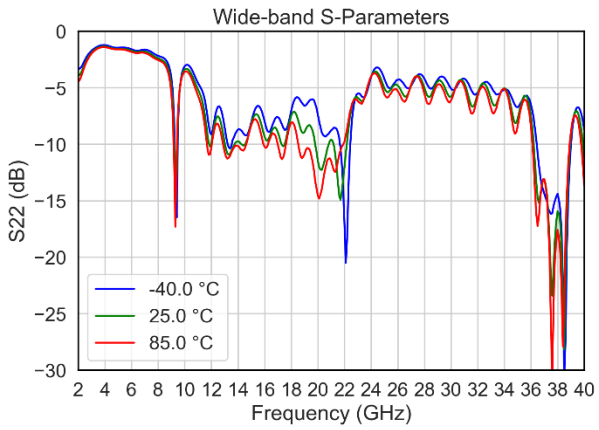
S21 measurements are de-embedded at QFN reference plans

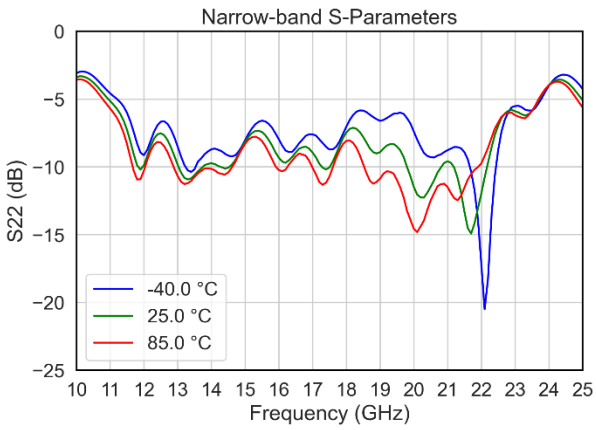












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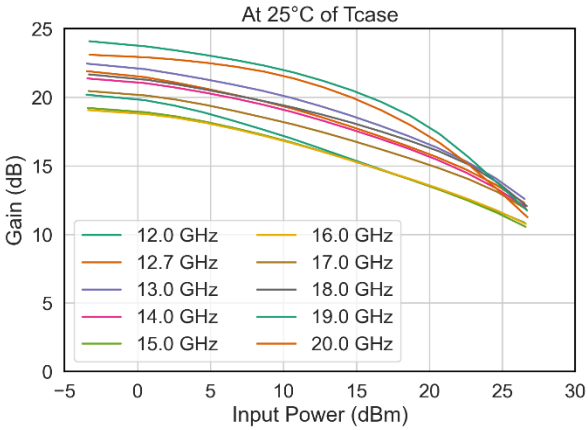
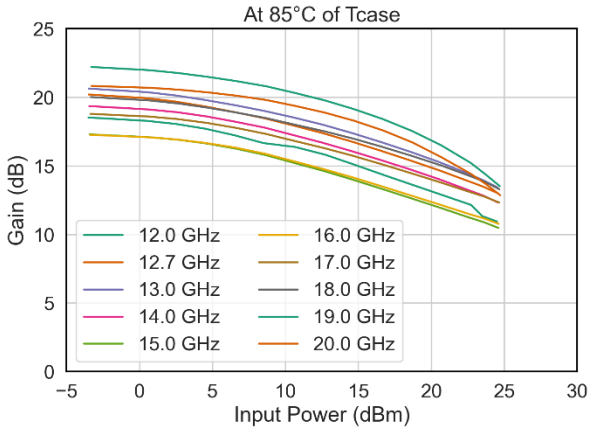
Typical Board Measurements: Large Signal Performances

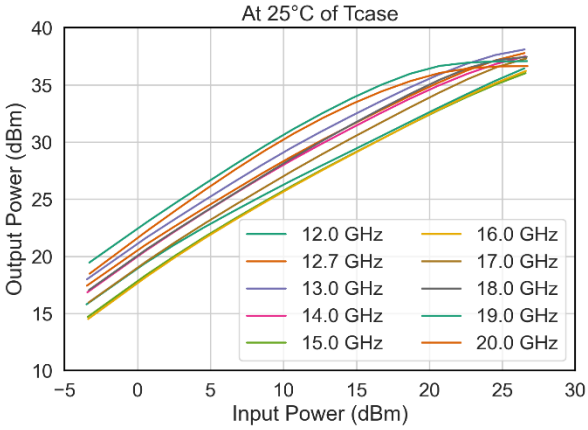
Performance vs. frequency and temperature
Test conditions: CW, Vd = 20V, Idq = 216mA, Tcase = 25°C (left) / 85°C (right)

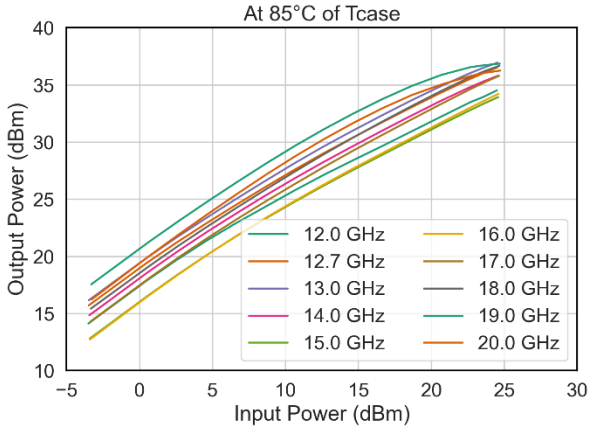
Gain vs. Input Power



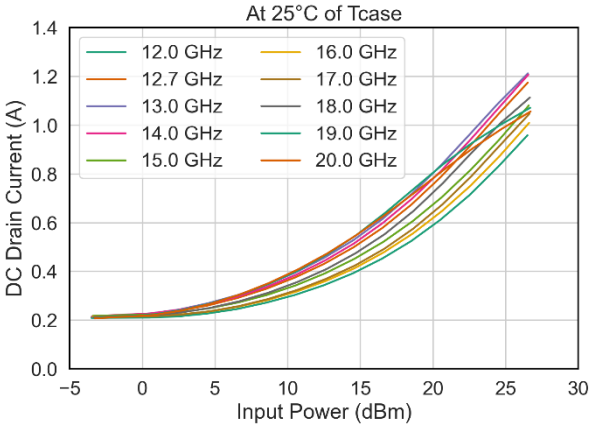


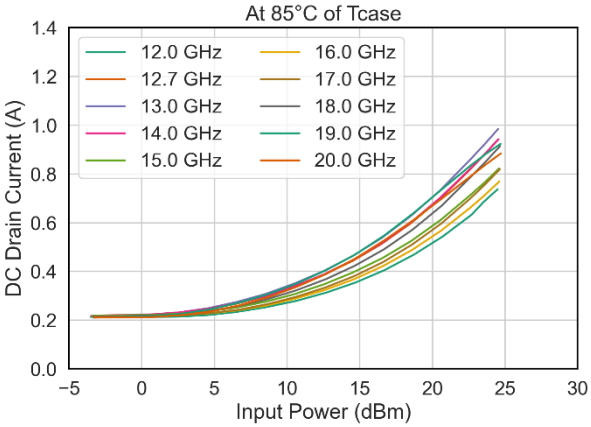
Output Power vs. Input Power





DC Current vs. Input Power





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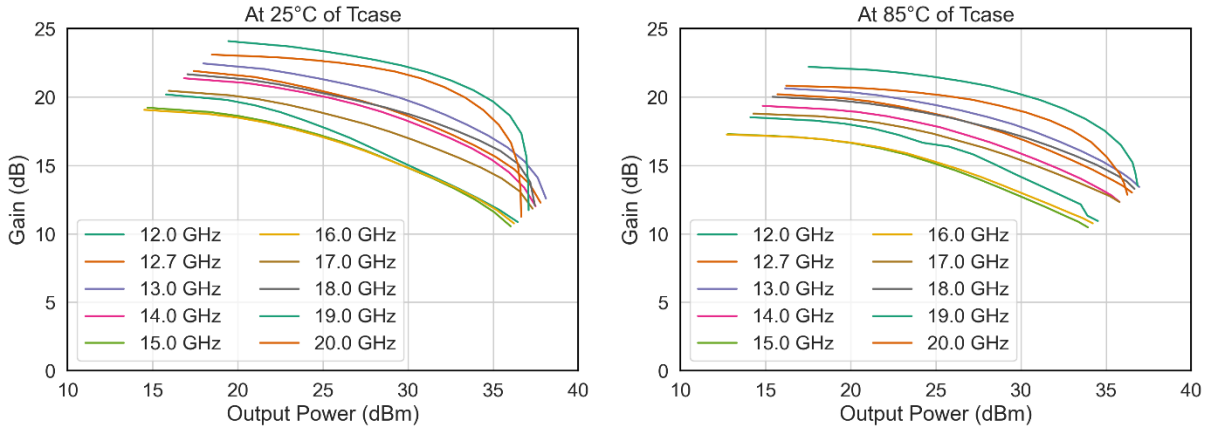
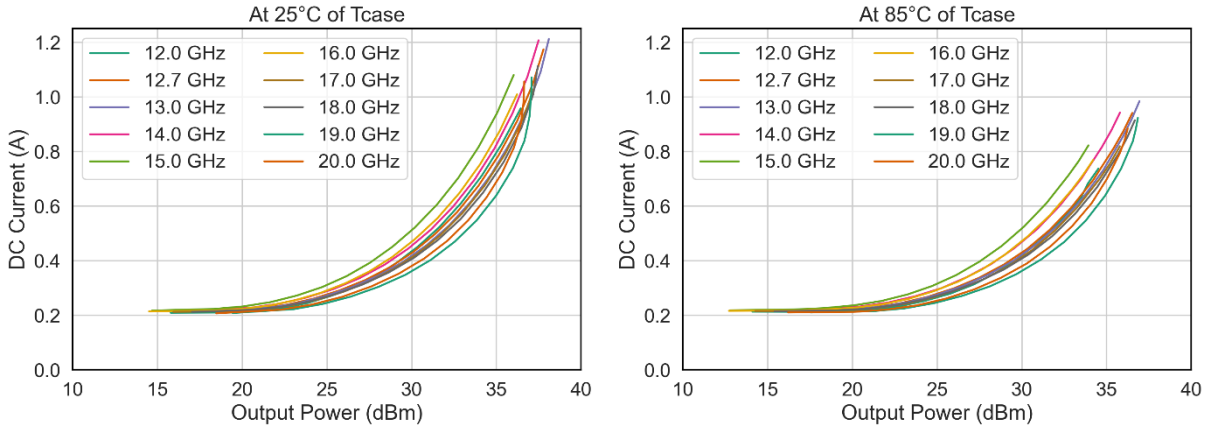
Typical Board Measurements: Large Signal Performances

Performance vs. frequency and temperature
Test conditions: CW, Vd = 20V, Idq = 216mA, Tcase = 25°C (left) / 85°C (right)

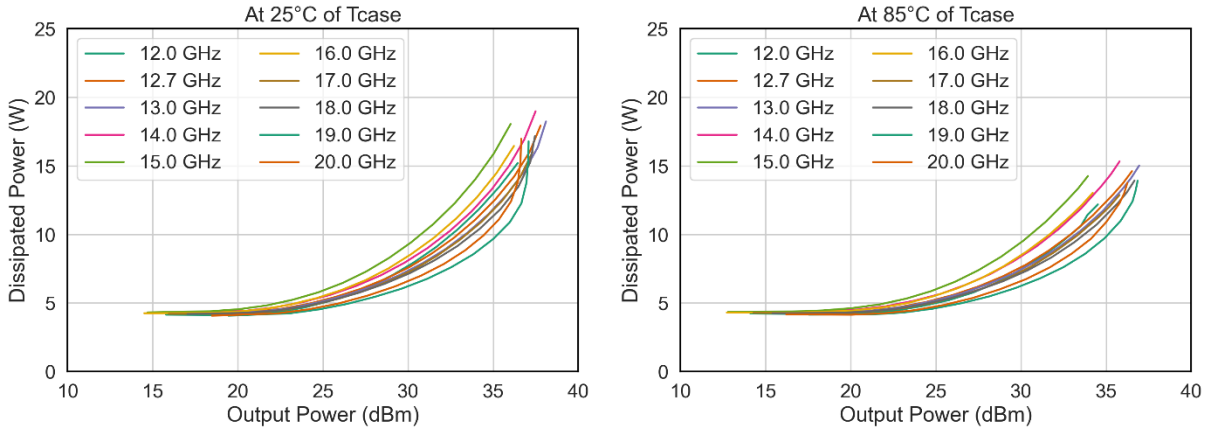
Gain vs. Output Power



DC Current vs. Output Power



Dissipated Power vs. Output Power



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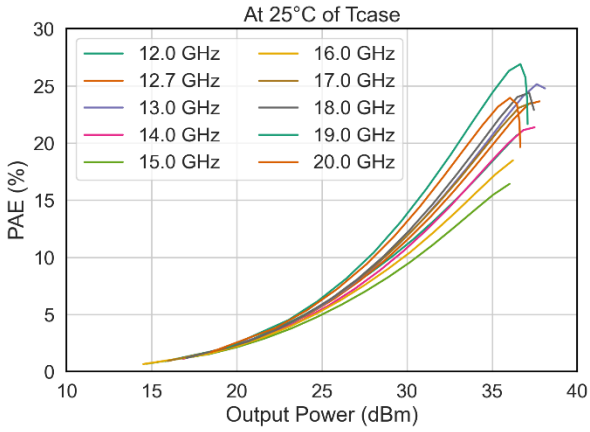
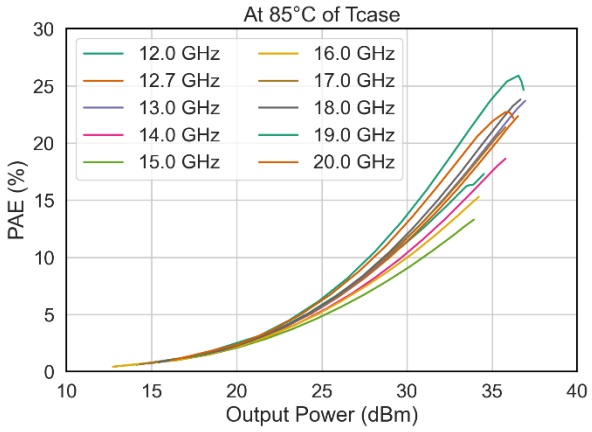
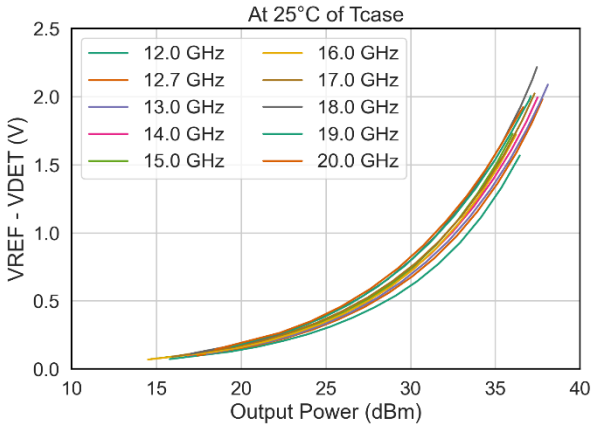
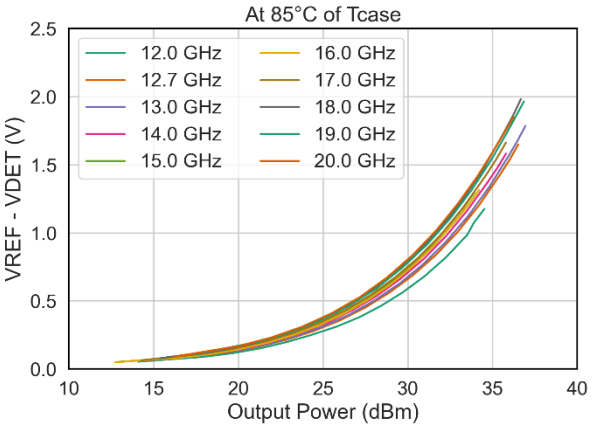
PAE vs. Output Power





Voltage Detection vs. Output Power





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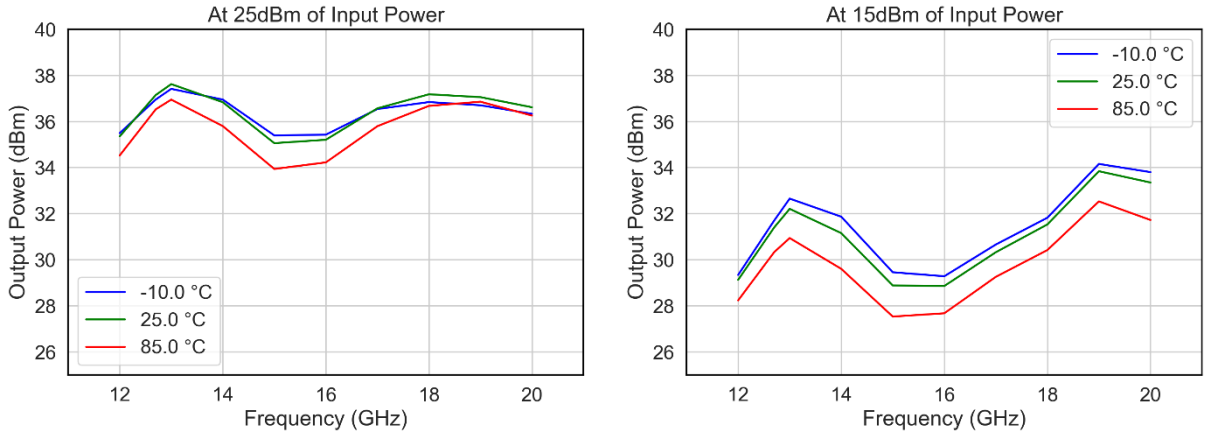
Typical Board Measurements: Large Signal Performances

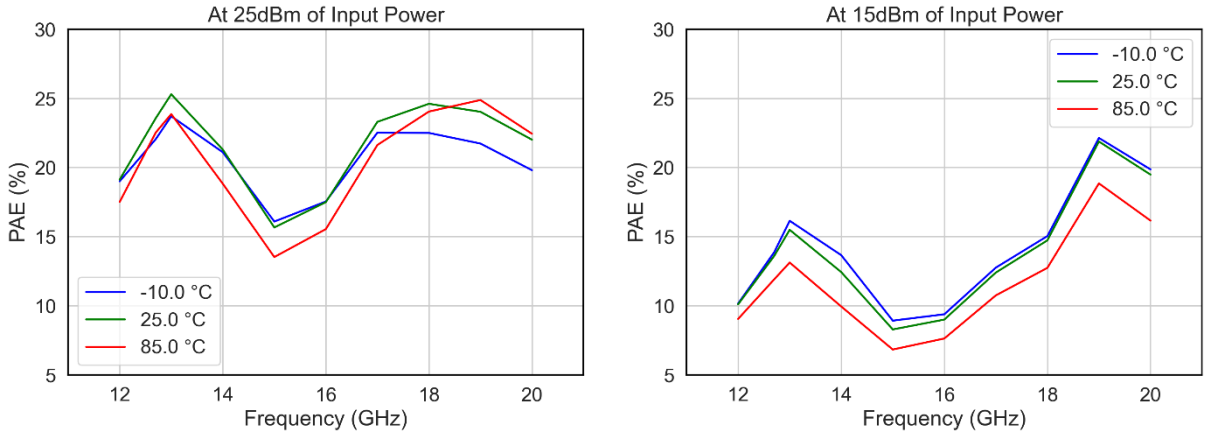
Performance vs. Frequency and Temperature

Test conditions: CW, Vd = 20V, Idq = 216mA, Tcase = -10°C / 25°C / 85°C for 25dBm (left) / 15dBm (right) of input power i.e. 6dB of output power back-off

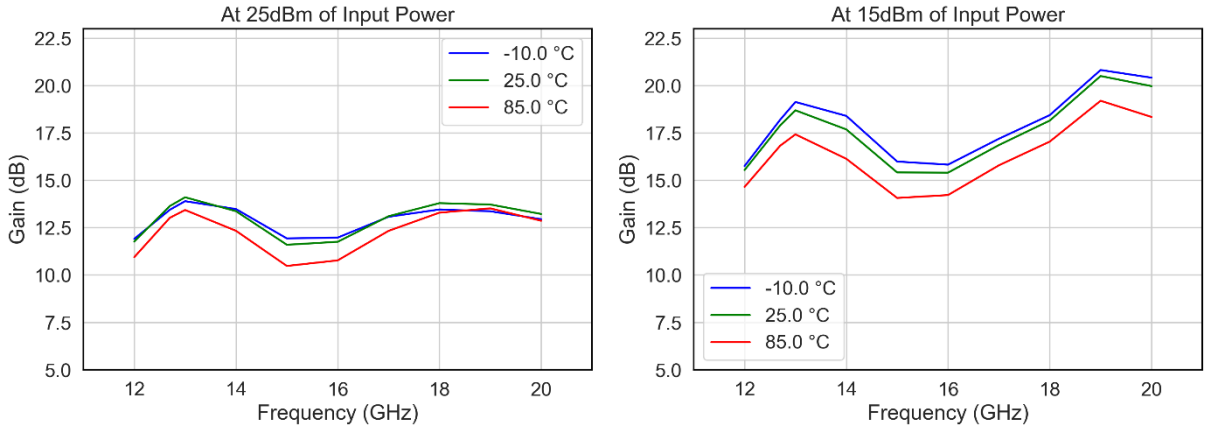
Output Power vs. Frequency



PAE vs. Frequency



Gain vs. Frequency



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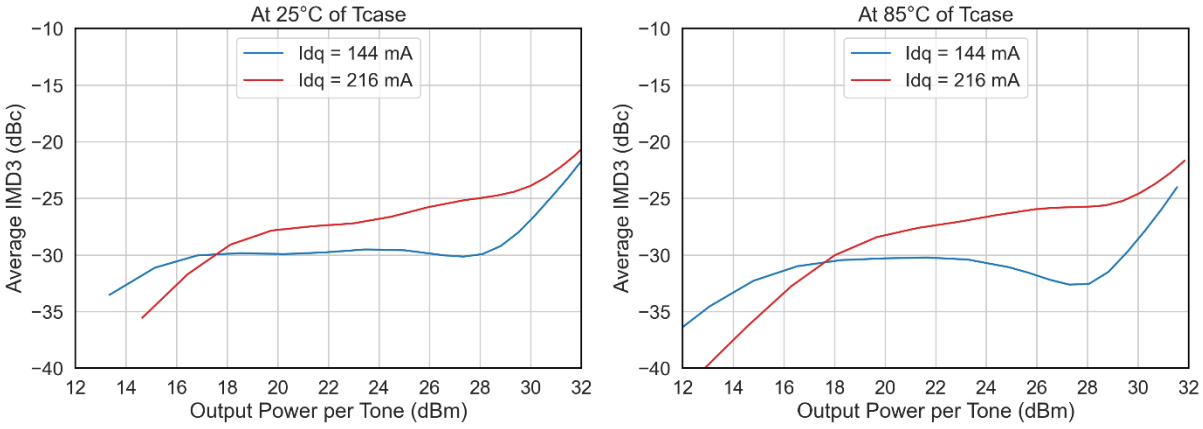
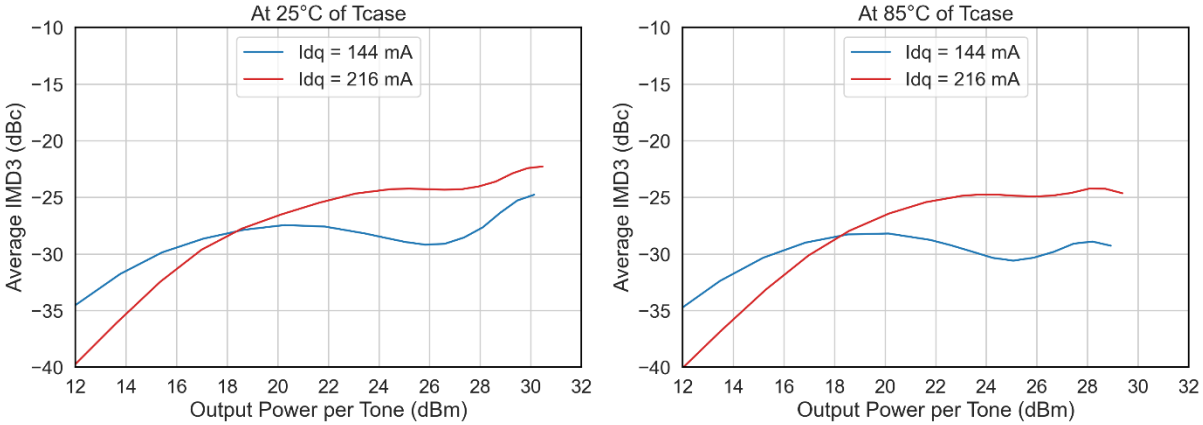
Typical Board Measurements: Intermodulation Distortion

Test conditions: CW, Vd = 20V, **Δf = 10MHz**

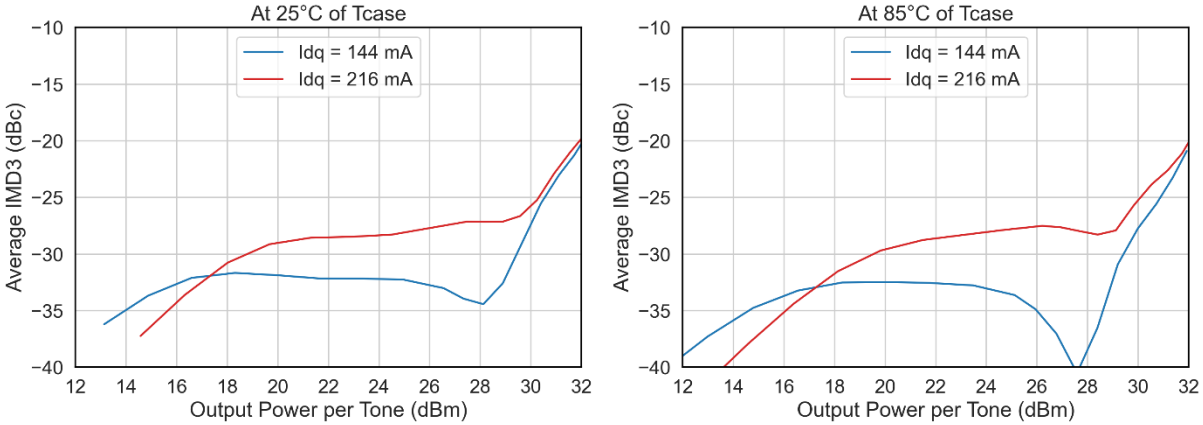
IMD3 vs. output power per tone at 13GHz center frequency



IMD3 vs. output power per tone at 15GHz center frequency



IMD3 vs. output power per tone at 18GHz center frequency



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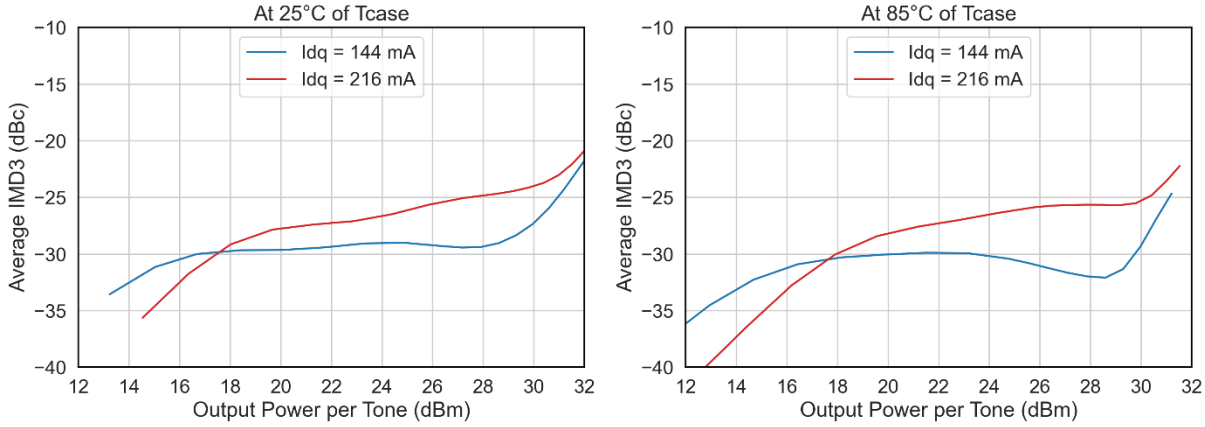
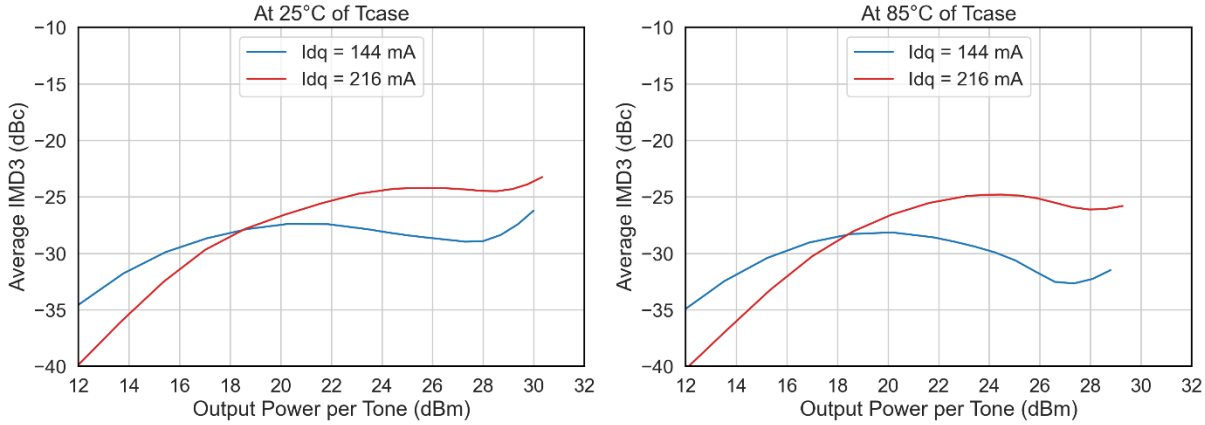
Typical Board Measurements: Intermodulation Distortion

Test conditions: CW, Vd = 20V, **Δf = 100MHz**

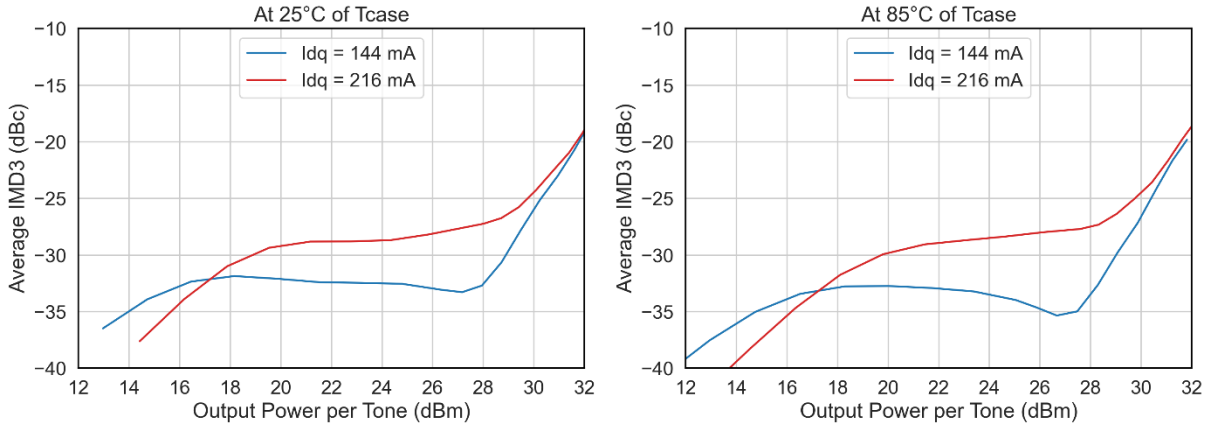
IMD3 vs. output power per tone at 13GHz center frequency



IMD3 vs. output power per tone at 15GHz center frequency



IMD3 vs. output power per tone at 18GHz center frequency



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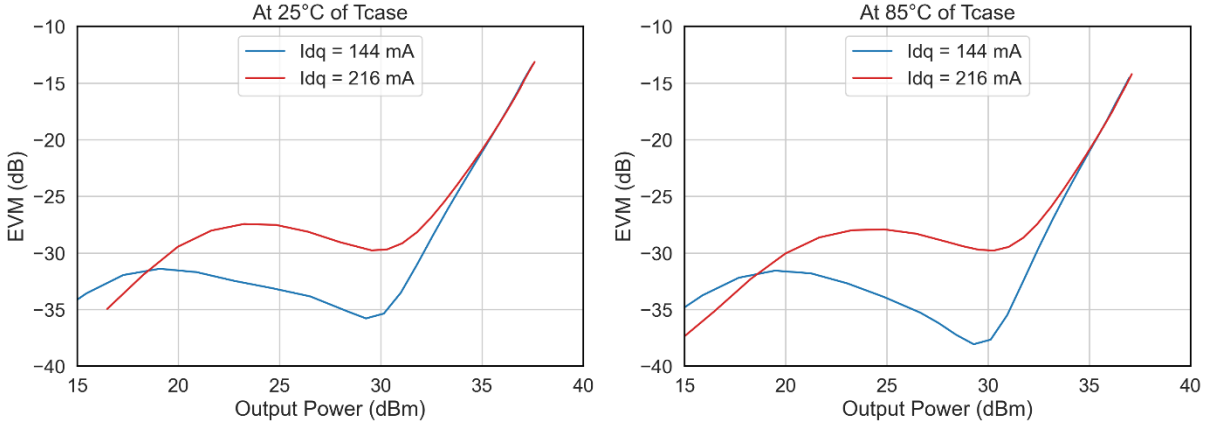
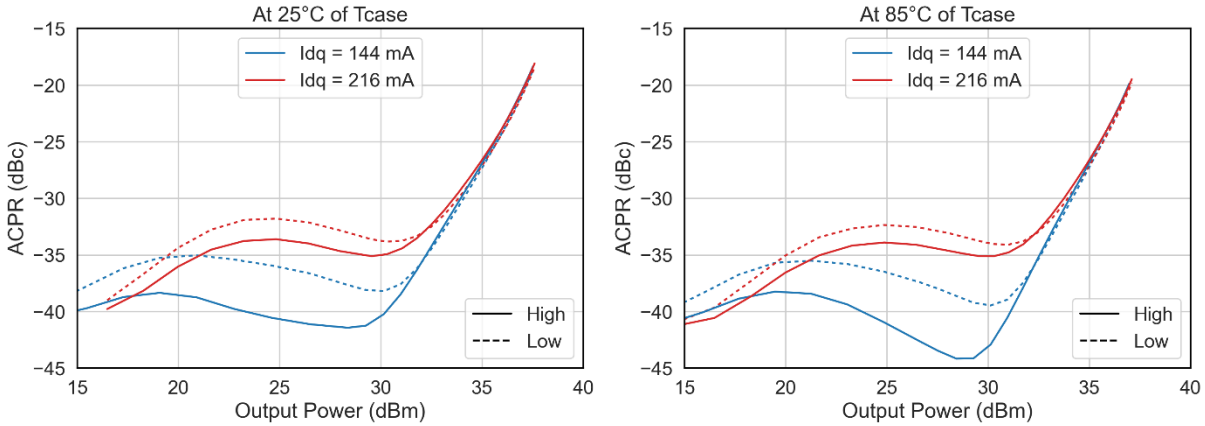
Typical Board Measurements: Modulation Measurements

Test conditions: Vd = 20V, 256QAM, f_C = **13GHz**, BW = 200MHz, Roll-off = 0.2, PAPR = 7.2dB

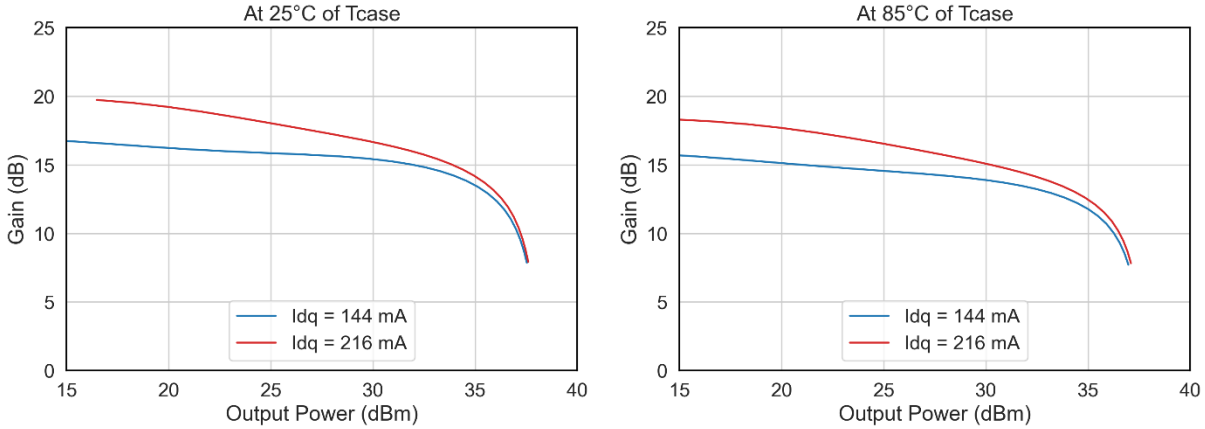
Error Vector Magnitude vs. Output Power



Adjacent Channel Power Ratio vs. Output Power



Gain vs. Output Power



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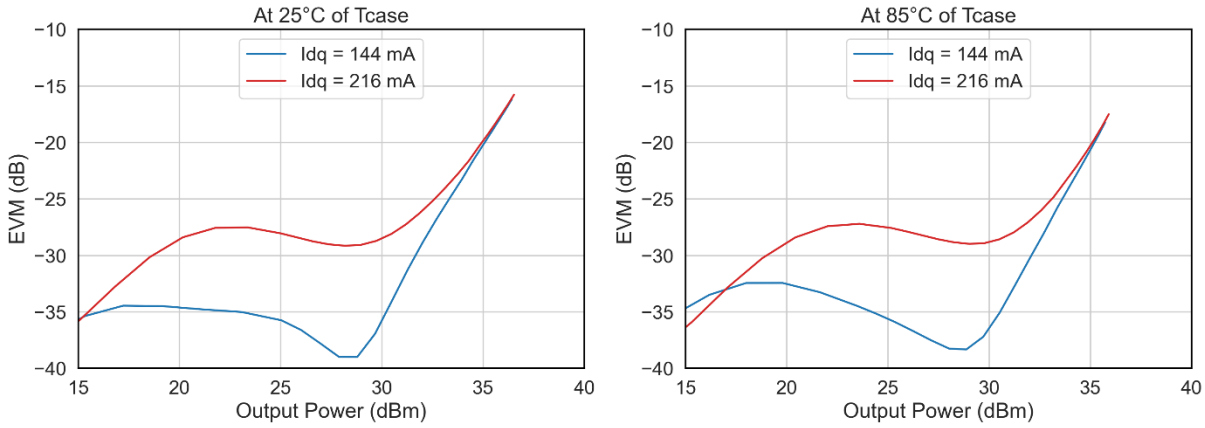
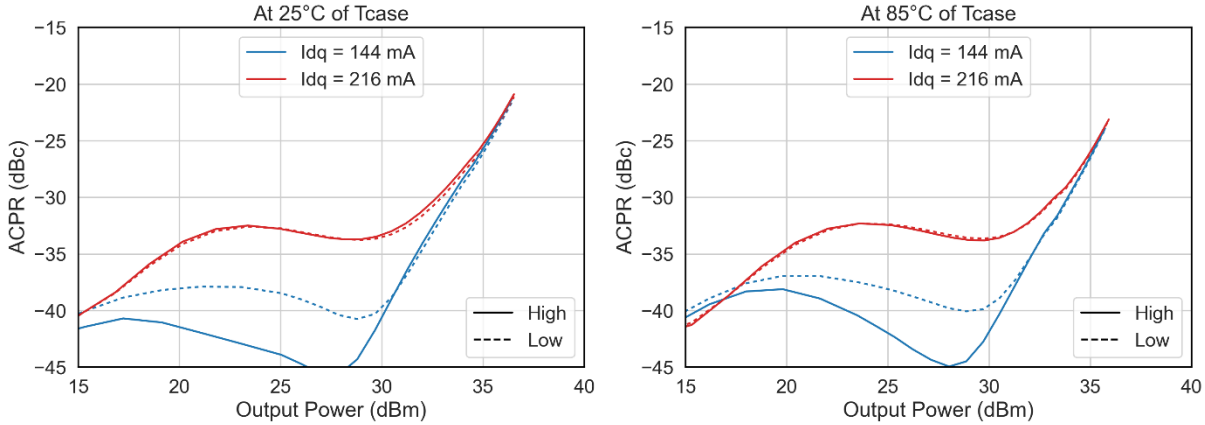
Typical Board Measurements: Modulation Measurements

Test conditions: Vd = 20V, 256QAM, f_C = **15GHz**, BW = 200MHz, Roll-off = 0.2, PAPR = 7.2dB

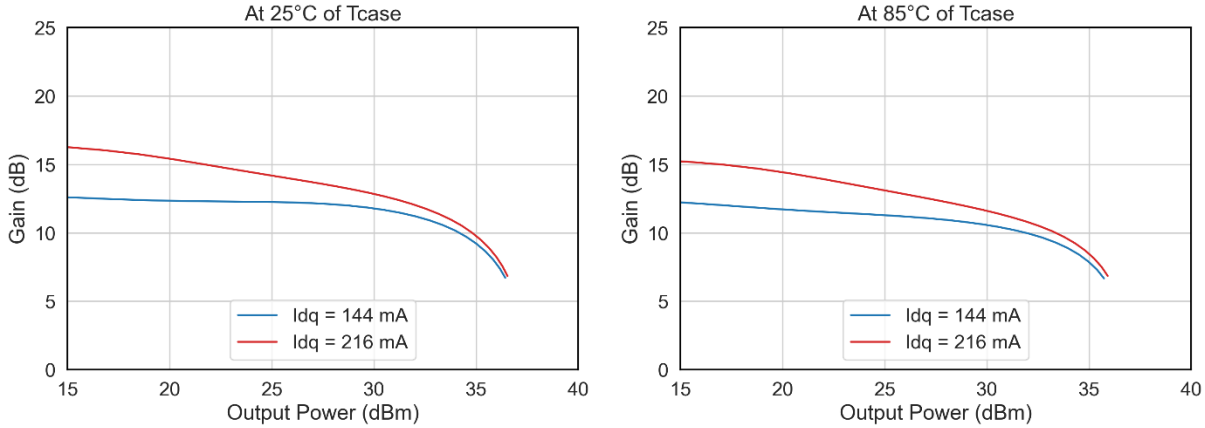
Error Vector Magnitude vs. Output Power



Adjacent Channel Power Ratio vs. Output Power



Gain vs. Output Power



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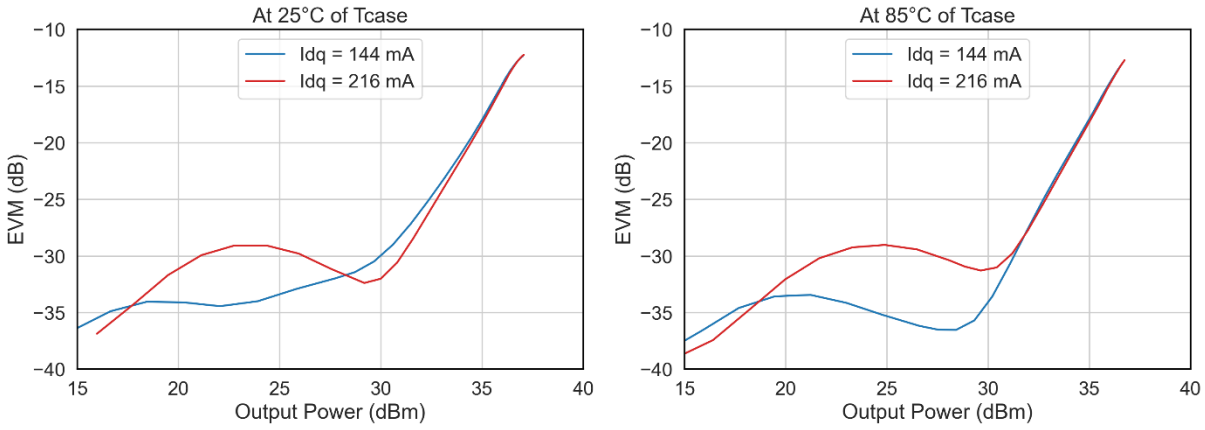
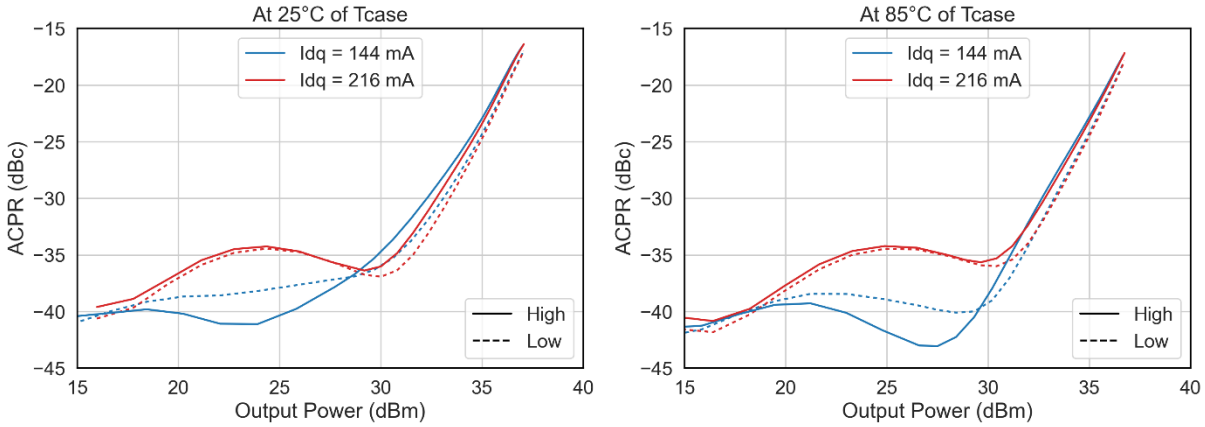
Typical Board Measurements: Modulation Measurements

Test conditions: Vd = 20V, 256QAM, f_C = **18GHz**, BW = 200MHz, Roll-off = 0.2, PAPR = 7.2dB

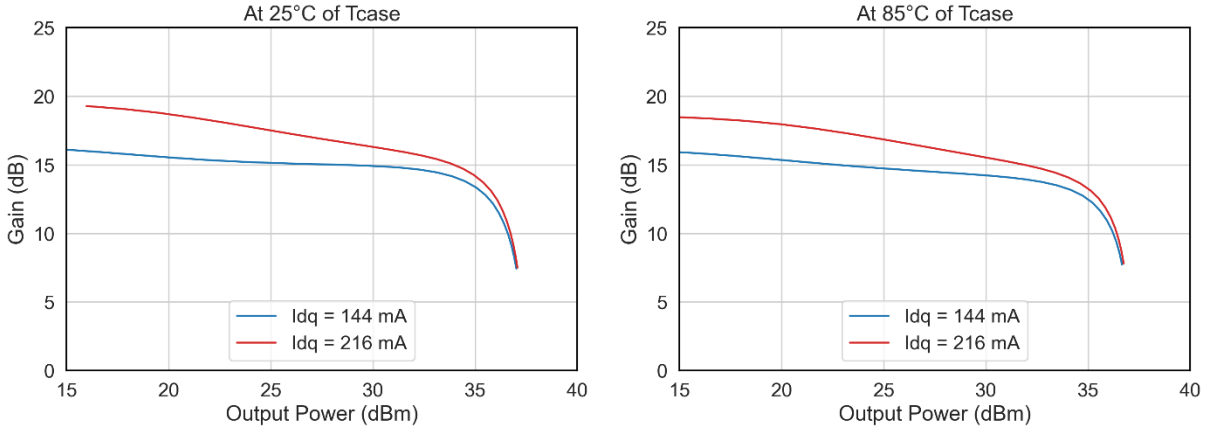
Error Vector Magnitude vs. Output Power



Adjacent Channel Power Ratio vs. Output Power



Gain vs. Output Power



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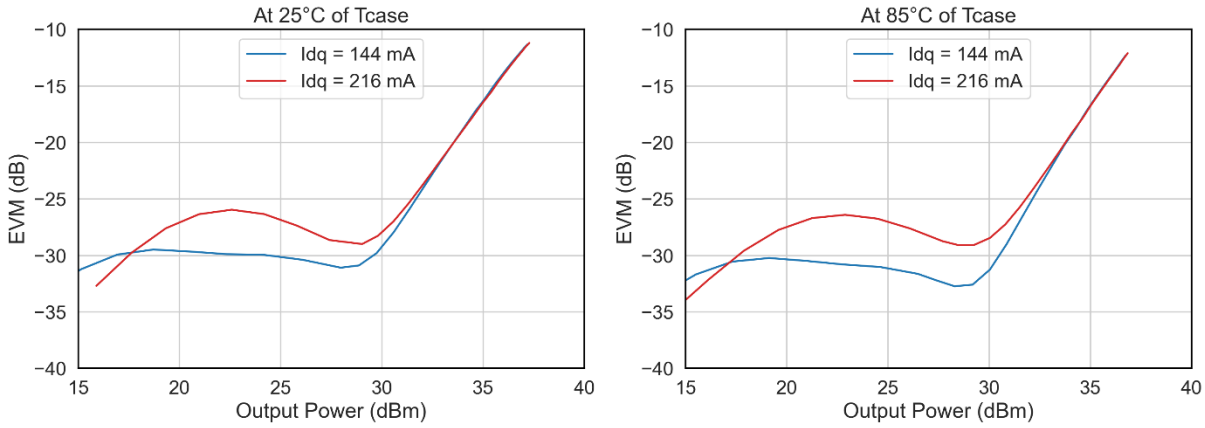
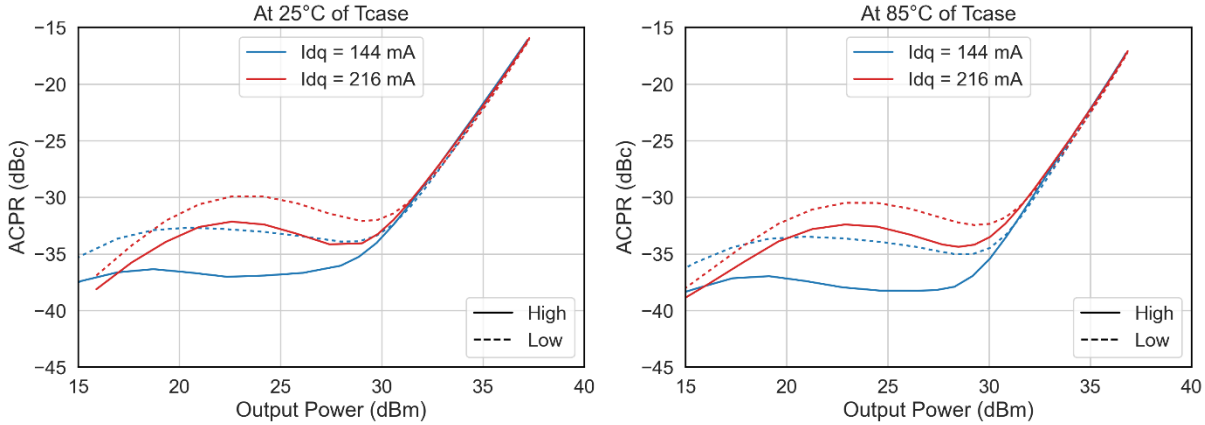
Typical Board Measurements: Modulation Measurements

Test conditions: Vd = 20V, 256QAM-OFDM, f_C = **13GHz**, BW = 200MHz, Flat tone, PAPR = 9.4dB

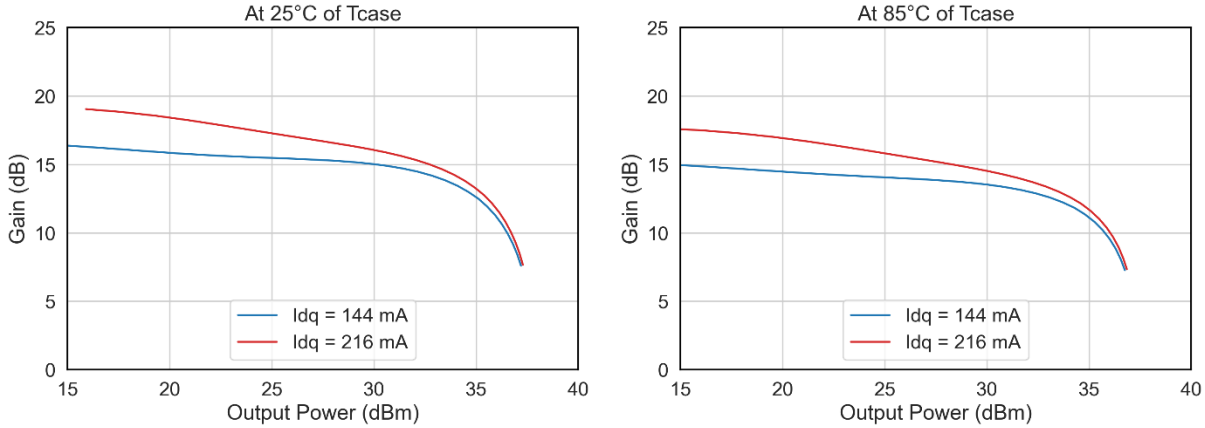
Error Vector Magnitude vs. Output Power



Adjacent Channel Power Ratio vs. Output Power



Gain vs. Output Power



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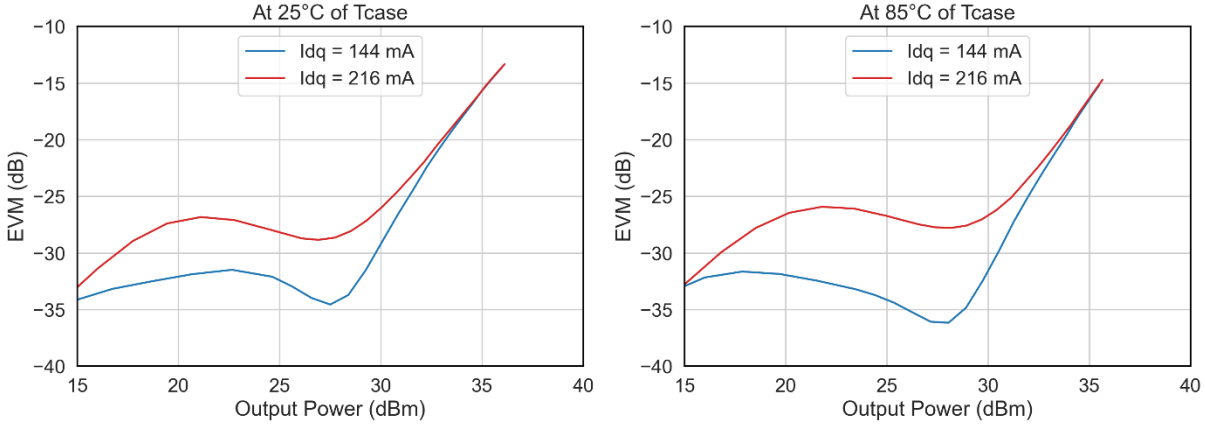
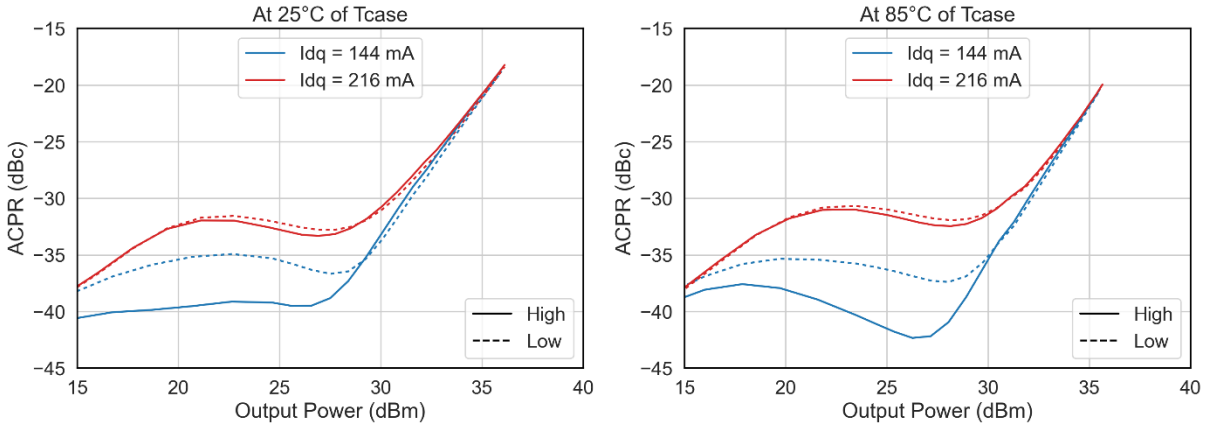
Typical Board Measurements: Modulation Measurements

Test conditions: Vd = 20V, 256QAM-OFDM, f_C = **15GHz**, BW = 200MHz, Flat tone, PAPR = 9.4dB

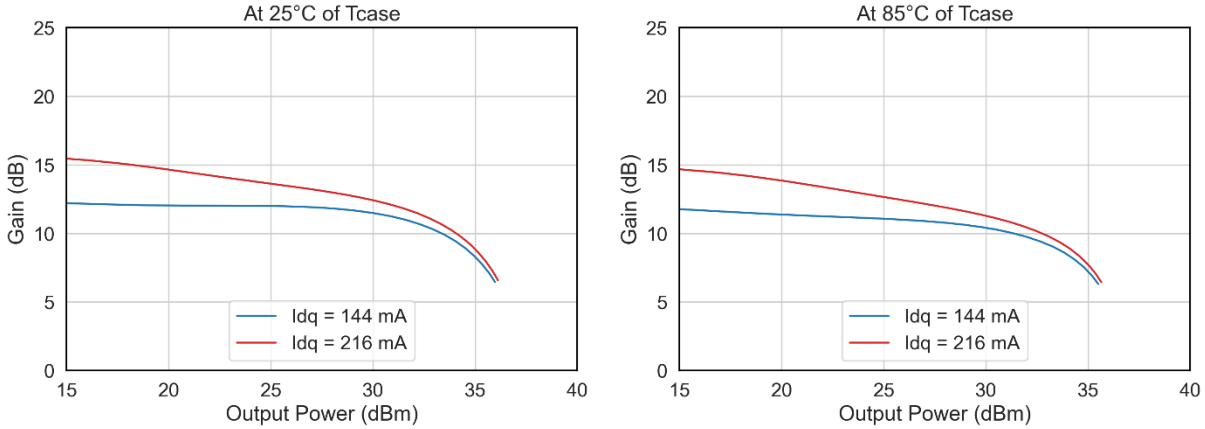
Error Vector Magnitude vs. Output Power



Adjacent Channel Power Ratio vs. Output Power



Gain vs. Output Power



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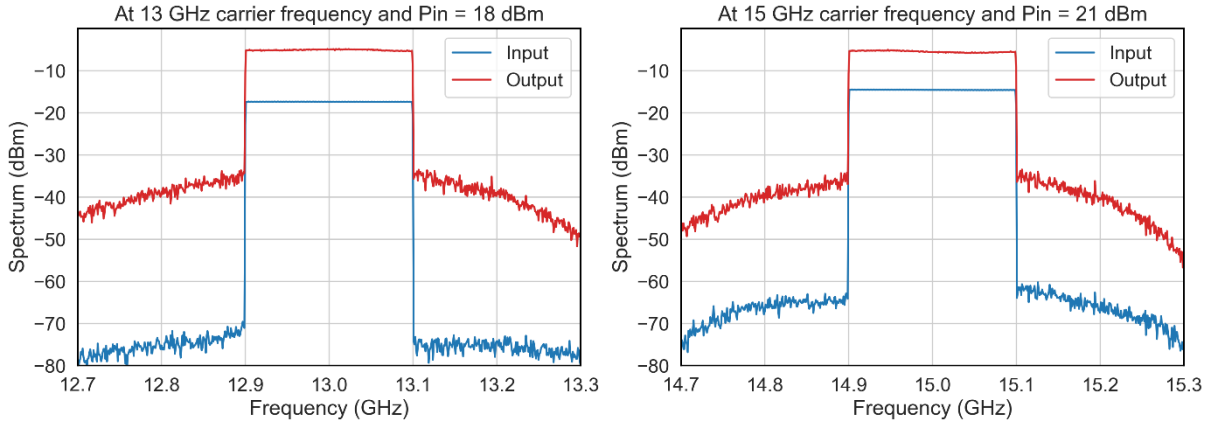
Typical Board Measurements: Modulation Measurements

Test conditions: Vd = 20V, Idq = 144mA, Tcase = 85°C, 256QAM-OFDM, BW = 200MHz, Flat tone, PAPR = 9.4dB

Input and Output Spectrum vs. Frequency



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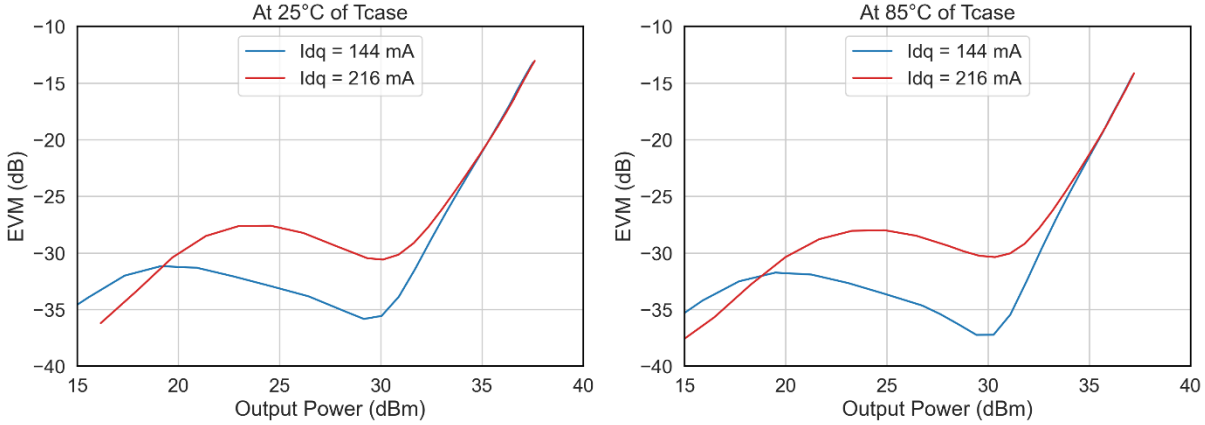
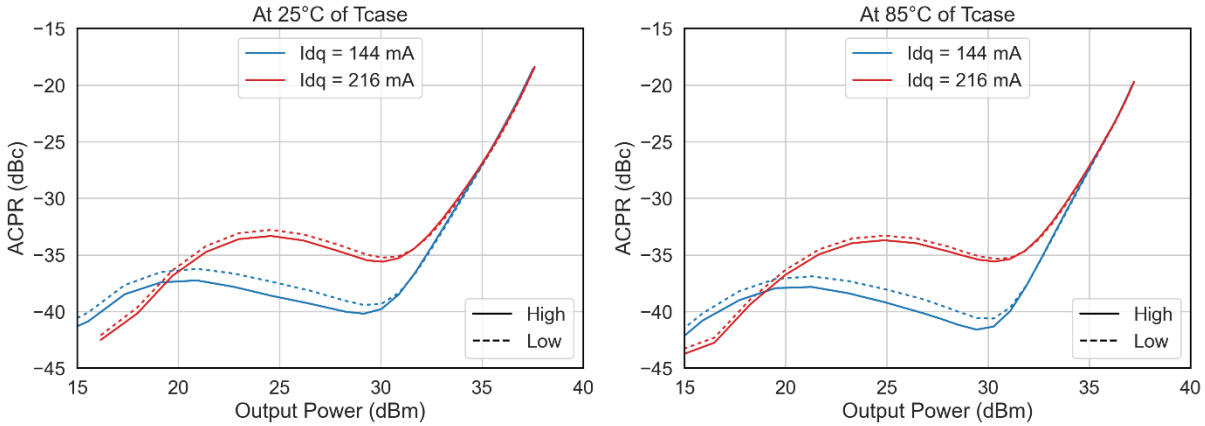
Typical Board Measurements: Modulation Measurements

Test conditions: Vd = 20V, 1024QAM, f_C = **13GHz**, BW = 56MHz, Roll-off = 0.2, PAPR = 7.3dB

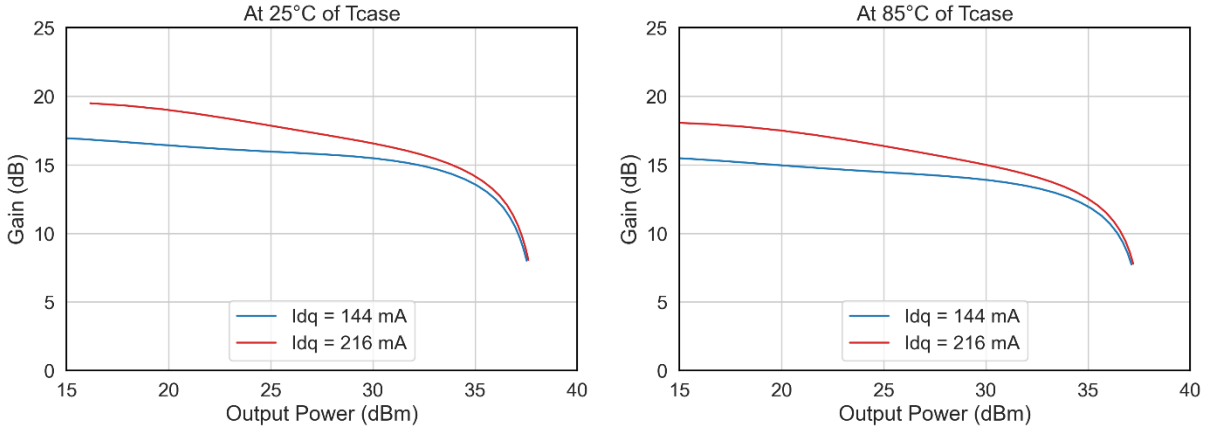
Error Vector Magnitude vs. Output Power



Adjacent Channel Power Ratio vs. Output Power



Gain vs. Output Power



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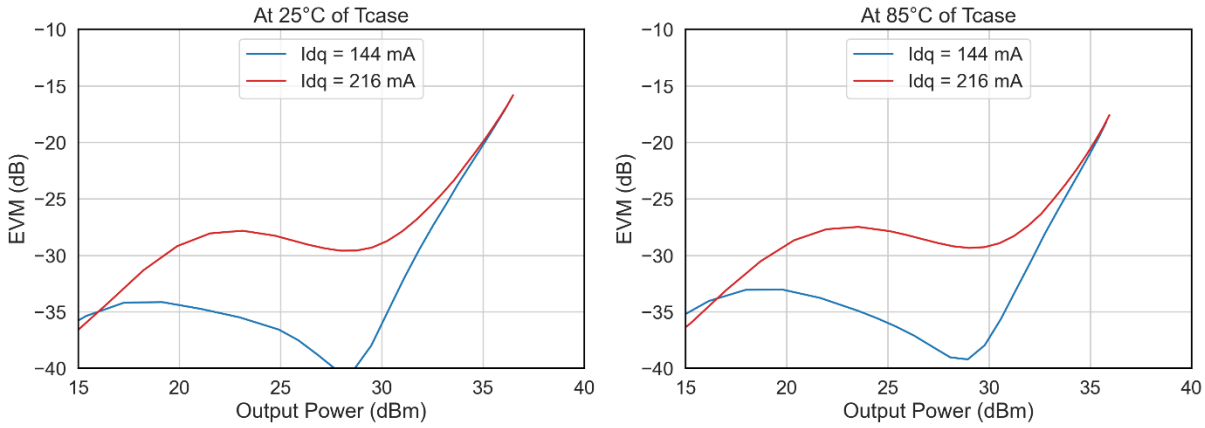
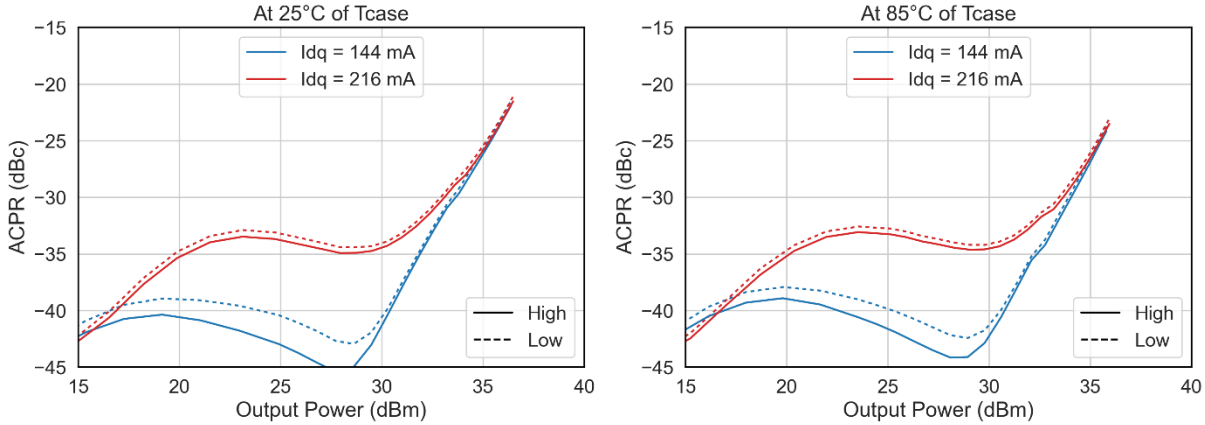
Typical Board Measurements: Modulation Measurements

Test conditions: Vd = 20V, 1024QAM, f_C = **15GHz**, BW = 56MHz, Roll-off = 0.2, PAPR = 7.3dB

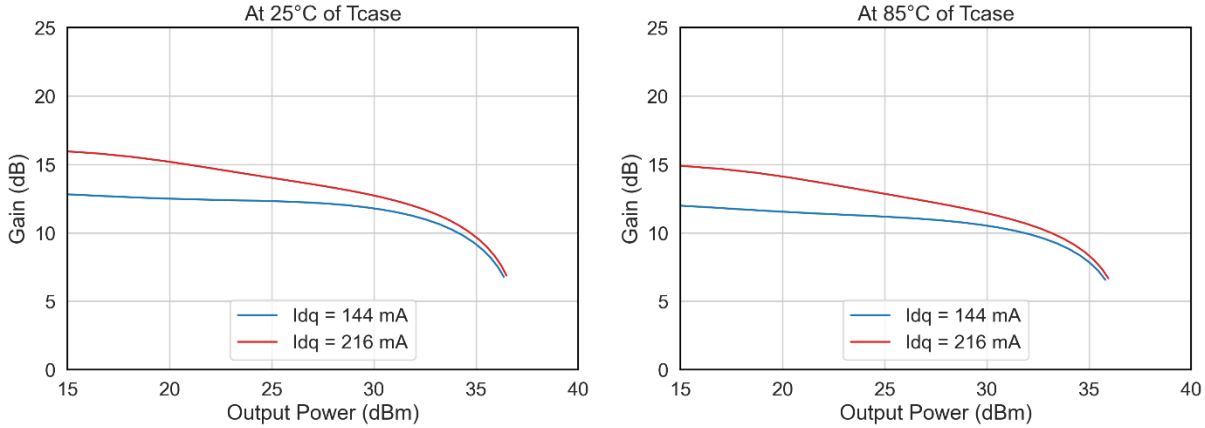
Error Vector Magnitude vs. Output Power



Adjacent Channel Power Ratio vs. Output Power



Gain vs. Output Power



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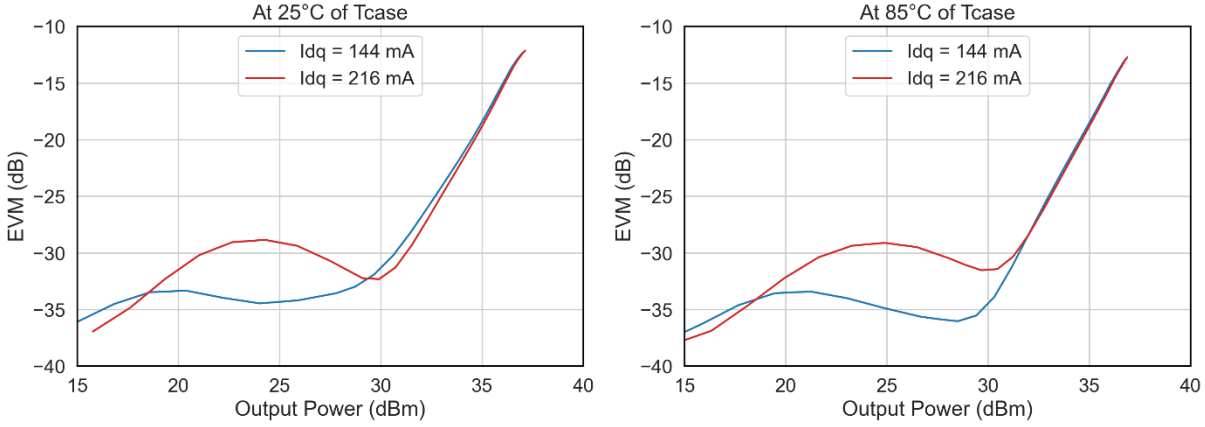
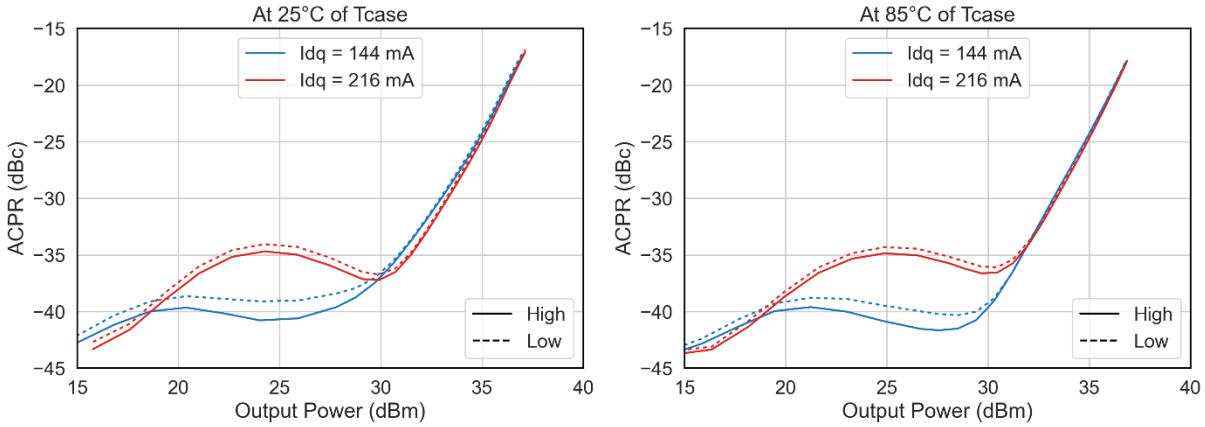
Typical Board Measurements: Modulation Measurements

Test conditions: Vd = 20V, 1024QAM, f_C = **18GHz**, BW = 56MHz, Roll-off = 0.2, PAPR = 7.3dB

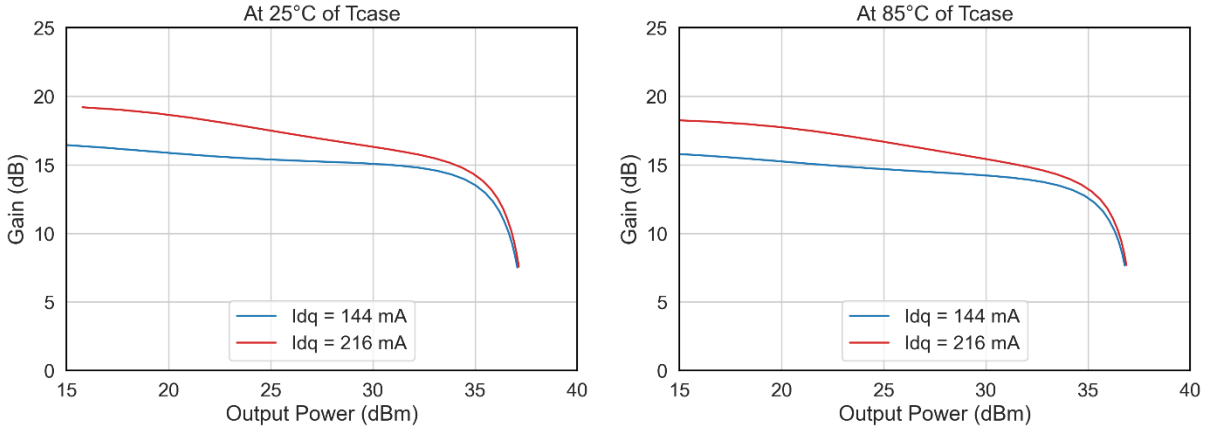
Error Vector Magnitude vs. Output Power



Adjacent Channel Power Ratio vs. Output Power



Gain vs. Output Power



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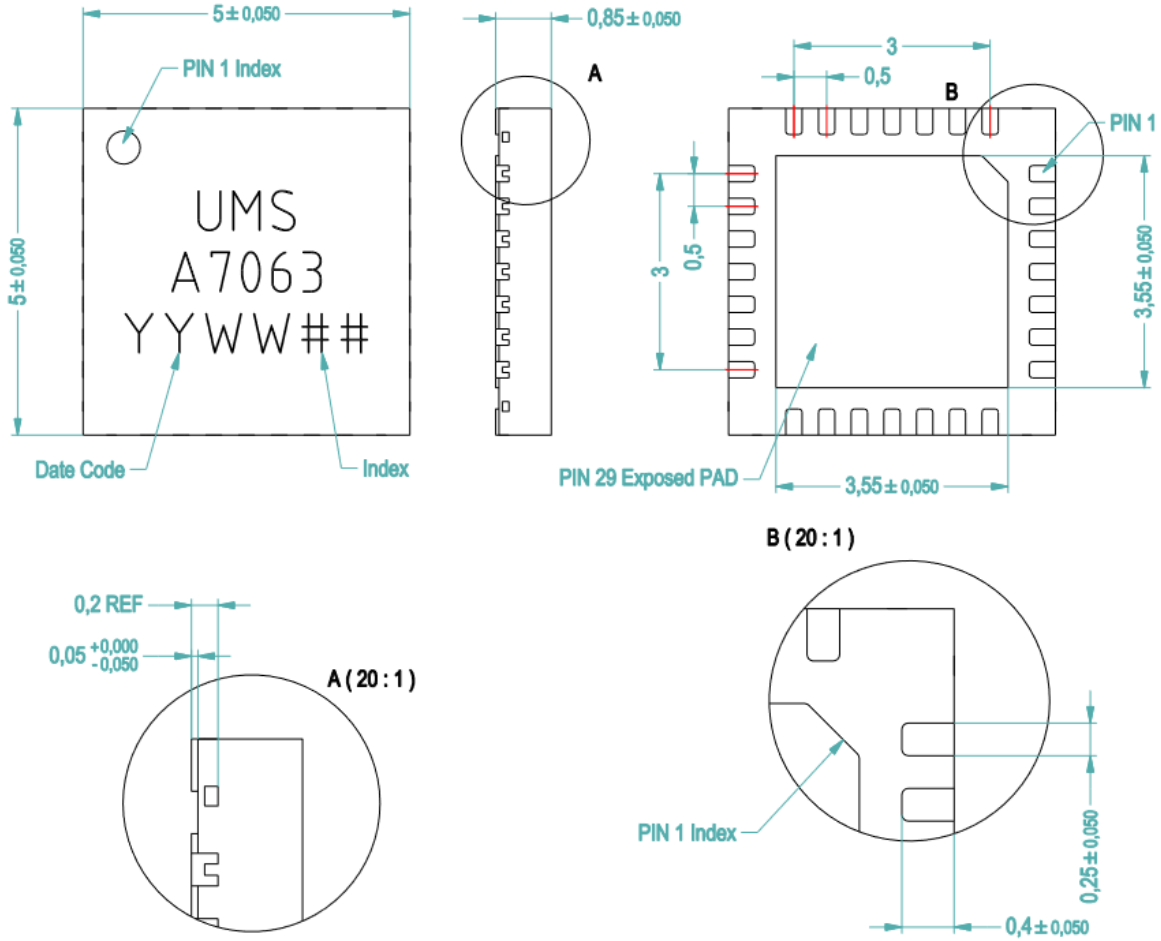
Package outline



Ni-Pd-Au-Ag Lead free (Green)		1- NC	11- VG2	21- VC
Units :	mm	2- NC	12- GND(1)	22- VDET
From the standard :	JEDEC MO-220	3- GND(1)	13- VD2	23- VD2
		4- RF IN	14- NC	24- GND(1)
		5- GND(1)	15- NC	25- VG2
		6- NC	16- NC	26- GND(1)
		7- NC	17- GND(1)	27- VD1
		8- VG1	18- RF OUT	28- VG1
		9- VD1	19- GND(1)	29- GND(1)
		10- GND(1)	20- VREF	

(1) It is strongly recommended to ground all pins marked “GND” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.
See application note AN0017 for details.

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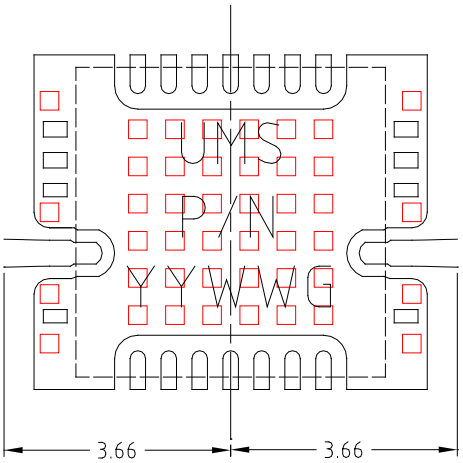
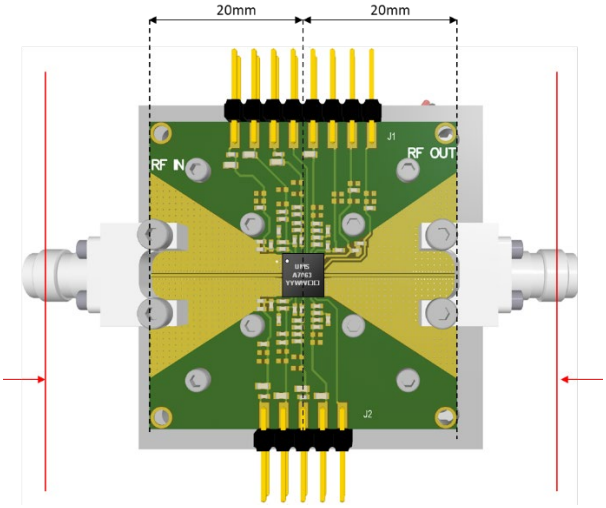
Definition of the Sij reference plans

Reference plans used for S21 measurements are symmetrical from the central axis of the package (see drawing on the right). Input and output reference plans are located at 3.66mm offset from the central axis. S21 parameter measurements include this given PCB pattern (see paragraph "Evaluation board").



Reference plans used for S11 and S22 measurements are symmetrical from the central axis of the package (see red lines in drawing on the right). Input and output reference plans are located at 20mm offset from the central axis. S11 and S22 measurements include this given PCB pattern, RF lines of the evaluation board and RF connectors.



ESD sensitivity

Parameter	Classification	Standard
Human Body Model (HBM)	1A	ANSI/ESDA/JEDEC - JS-001

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% Ni-Pd-Au-Ag
Moisture Sensitivity Level	MSL3

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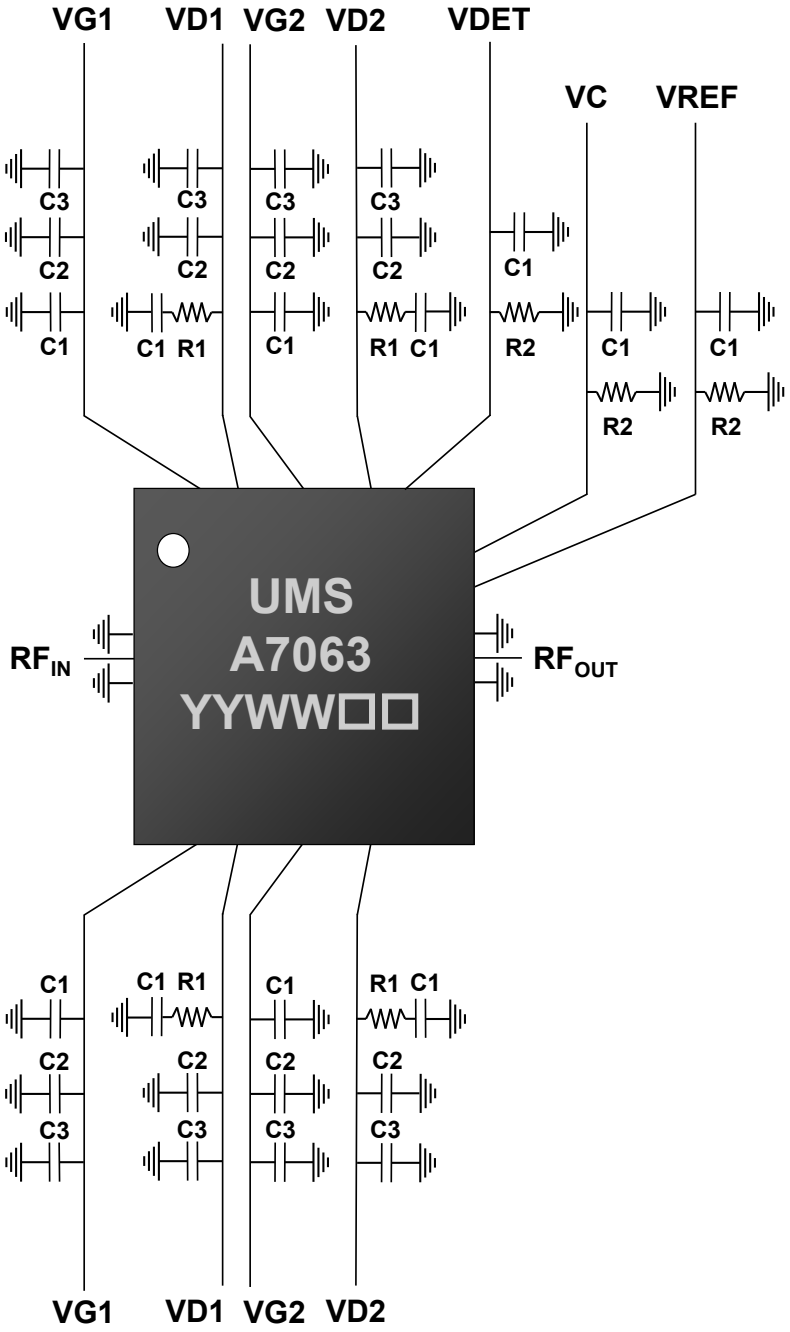
Recommended assembly plan



Bill of materials

Component	Value	Description
C1	100pF	CAP, 100pF ±10%, 50V, 0402
C2	10nF	CAP, 10nF ±10%, 50V, 0402
C3	1µF	CAP, 1µF ±10%, 50V, 0603
R1	10Ω	RES, 10Ω ±5%, 125mW, 0402
R2	10kΩ	RES, 10kΩ ±10%, 62mW, 0402

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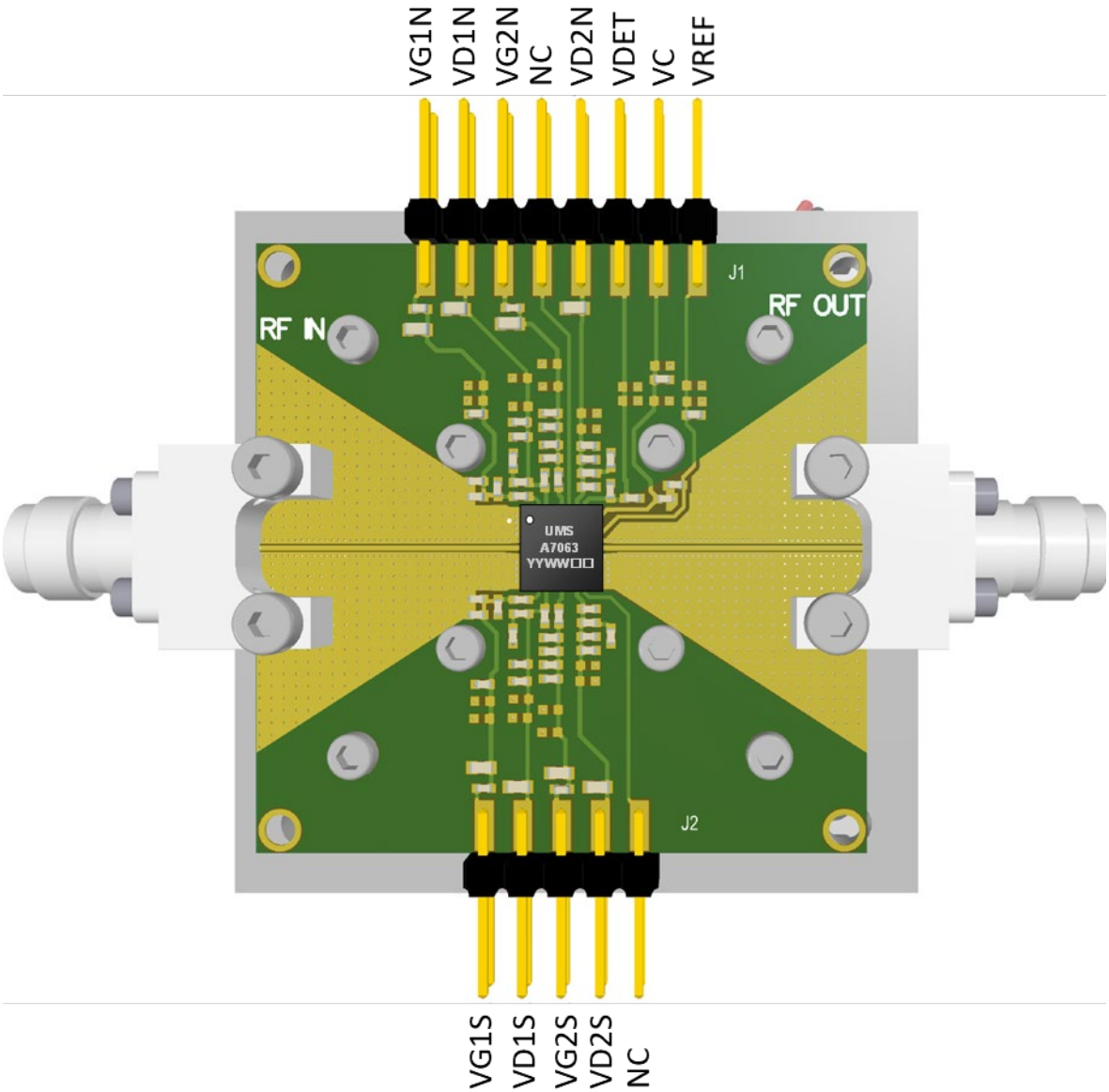
Evaluation board

- Compatible with the proposed footprint.
- Based on 8mils RO4003 or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF, 10nF and 1µF ±10% are recommended for all DC accesses.
- 10kΩ resistor in parallel with 100pF ±10% capacitors is recommended for VDET, VC and VREF detector pins.
- See application note AN0017 for details.



Note: All on-board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF pins.

The DC connections do not include any decoupling capacitor in package. Therefore, it is mandatory to provide external decoupling on the Printed Circuit Board, as close as possible to the package.

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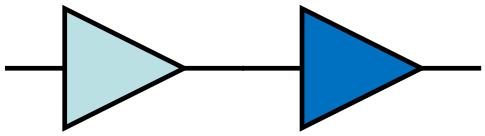
Recommended UMS Power Chain

The CHA7063-QCB is recommended with the CHA5266-QDG or CHA4253aQDG as driver.
Total Gain: 43dB
For more information about the CHA5266-QDG and CHA4253aQDG, see our web site
https://www.ums-rf.com



	Driver	HPA
Up to 16GHz	**CHA5266-QAG** **10-16GHz** **5V** **320mA**	**CHA7063-QCB** **12.7-20GHz** **20V** **216mA**
From 17GHz	**CHA4253aQQG** **17-24GHz** **4V** **230mA**	**CHA7063-QCB** **12.7-20GHz** **20V** **216mA**

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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques, involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 5x5 package:	CHA7063-QCB/XY	
	Stick: XY = 20	Tape & Reel: XY = 21

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